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# Introduction to Routers and LAN Switches

Session RST-101

# Prerequisites

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- **OSI Model**
- **Networking Fundamentals**

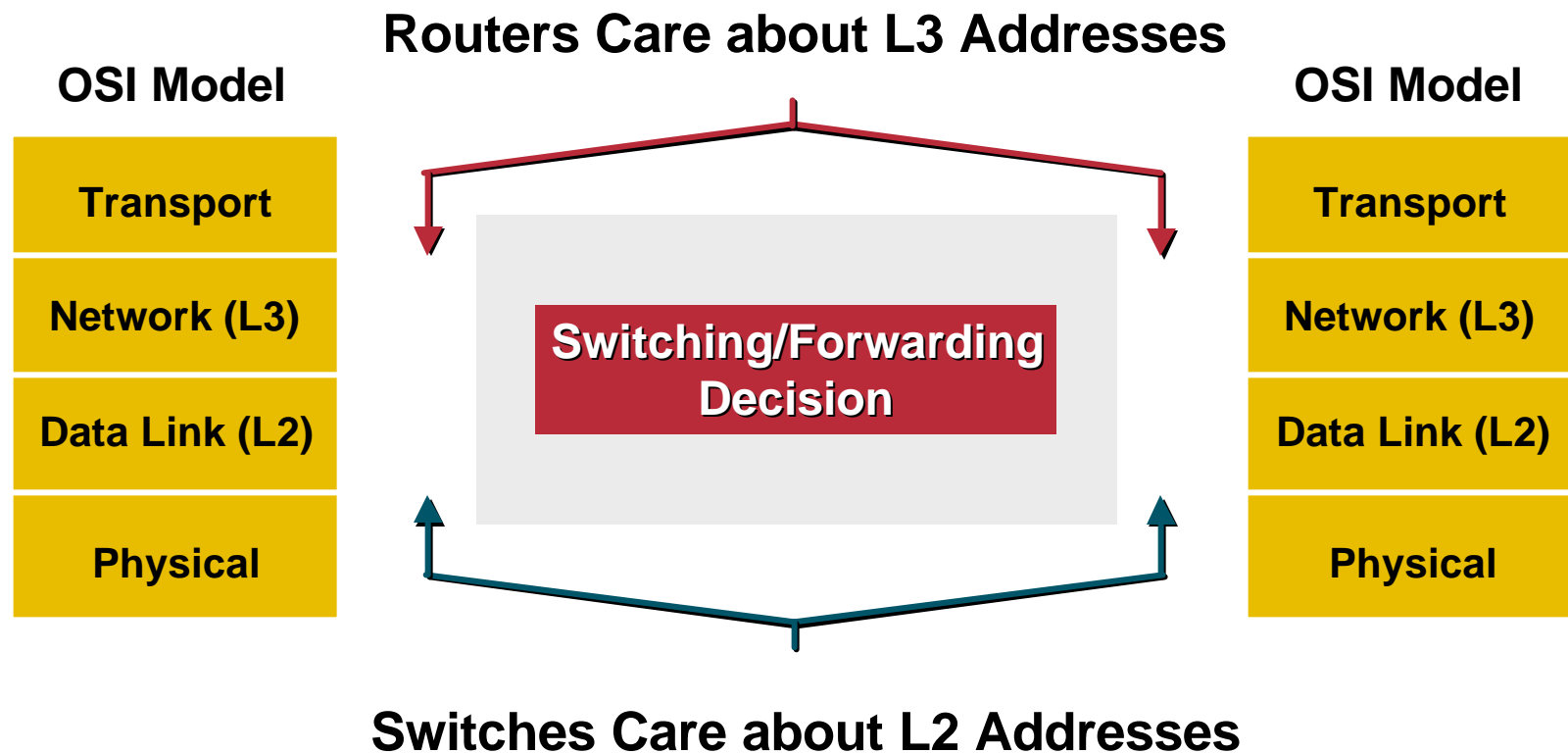
# Agenda

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- **Routers and LAN Switches**
- **Components of an Architecture**
- **Summary**

# Routers and LAN Switches

# What Are Routers and Switches

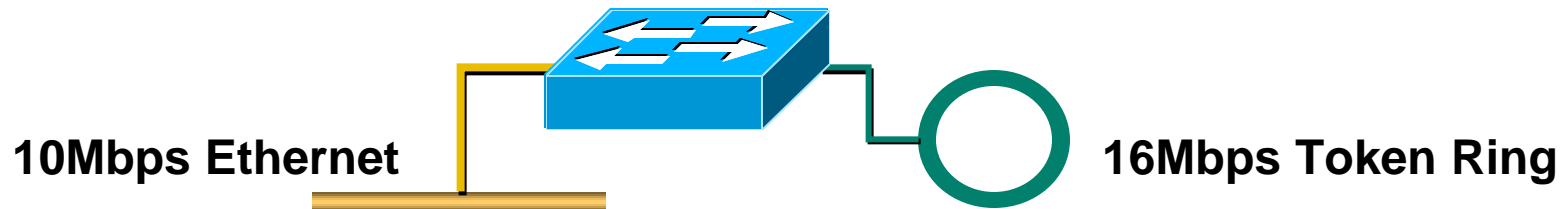


# Routers and Switches: Why Do We Need Them??

- Networks need to be connected to other networks



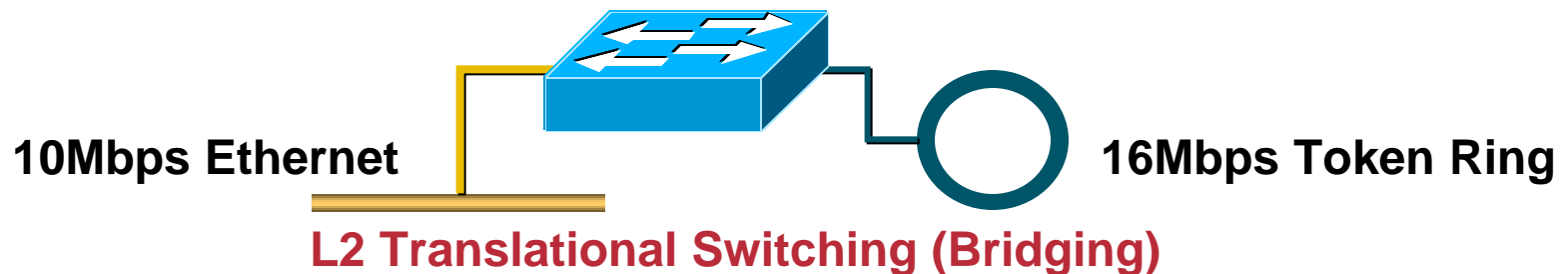
At L2 Same Media  $\leftrightarrow$  Media = **L2 Switching (Bridging)**  
(No Frame Changes, Speed Mismatches Accommodated)



At L2 Different Media  $\leftrightarrow$  Media = **L2 Translational Switching (Bridging)**  
(Frame Format Changes, Including Addresses, Flags, etc.)

# Routers and Switches: Why Do We Need Them??

- However...



In Both Examples, All Connected Devices Are Part of the Same Broadcast Domains, **There Is No Layer 3 Segmentation!!**  
This Becomes a Performance Issue Even in Medium Sized Networks

# Routers and Switches: Why Do We Need Them??

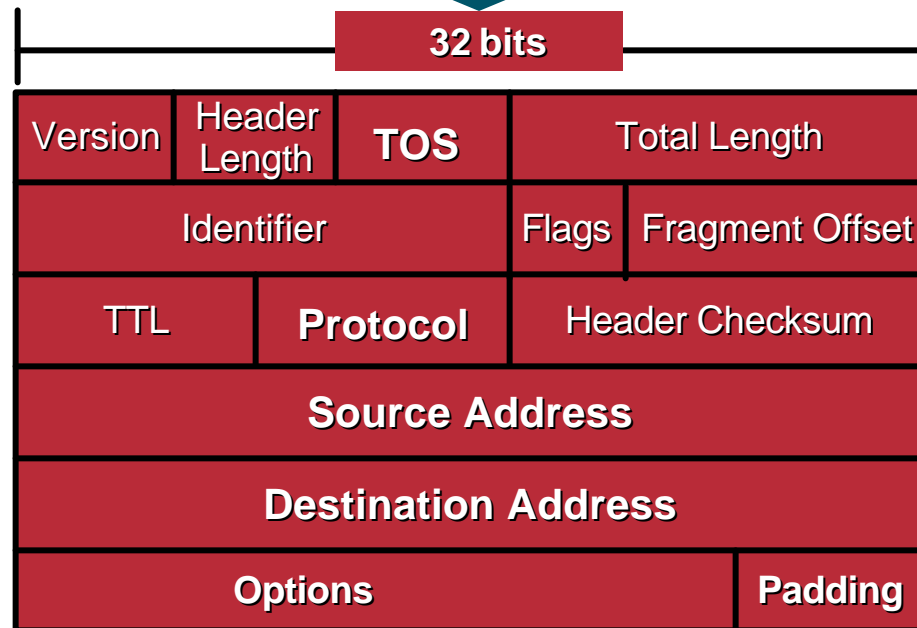
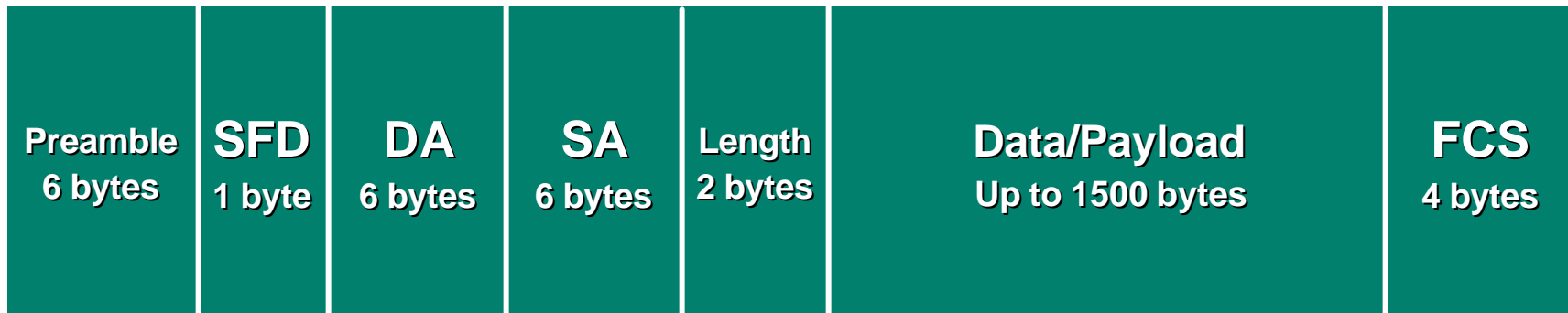
- **Networks need to be connected to other networks (LANs <> WANs, LANs<>LANs etc.)**
- **Networks don't scale well at L2 and need to be segmented at L3**

# What Are Routers and Switches

- **Routers and switches both make a decision as to how to handle packets or frames**
- **A frame is a L2 encapsulation**
- **A packet is a L3 encapsulation**

# Ethernet Frame and IP Packet

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# What Switches Really Do

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- **L2 classification**
- ***Switching Table* construction**
- **Other activities**

# Switches (Operationally)

- **Maintain/manipulate *Switching* information**
  - Record updates in MAC Table
- **Perform Layer 2 switching**
  - Compare Destination Address to “Learned” MAC Table
  - Check frame for errors
- **Management/billing (statistics)**
  - Interface statistics—Number of frames sent, error/collision counters, utilization

# Switches (Layer 2 Frame Functionally)

- **Switch frames**  
Layer 2 switching based on “*Switching*” information
- **Transmit frames**  
Access outbound memory (buffers) and physical media
- **Flood frames**  
Flood any unknown multicast/broadcast frames out all ports of the switch
- **Drop frames**  
Drop any frames that contain errors

# L2 Classification

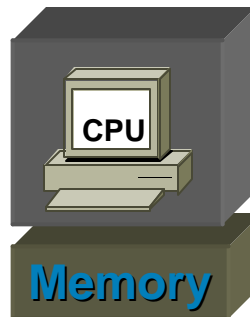
2

Look at **Destination Address** to determine which interface the frame will be switched through.

Default behavior of a switch is to flood unknown multicast/broadcast frames.

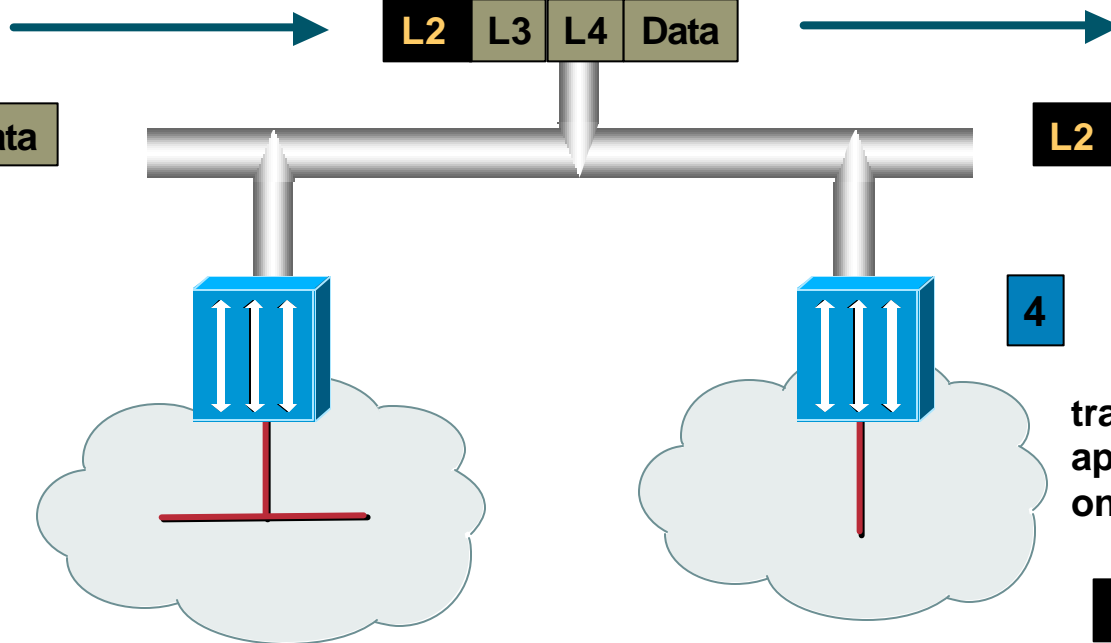
3

Frame stored in shared buffer



1

L2 provides local link addressing and data integrity validation



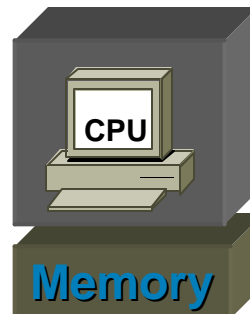
4

transmitted to the appropriate port based on the **Switching Table**

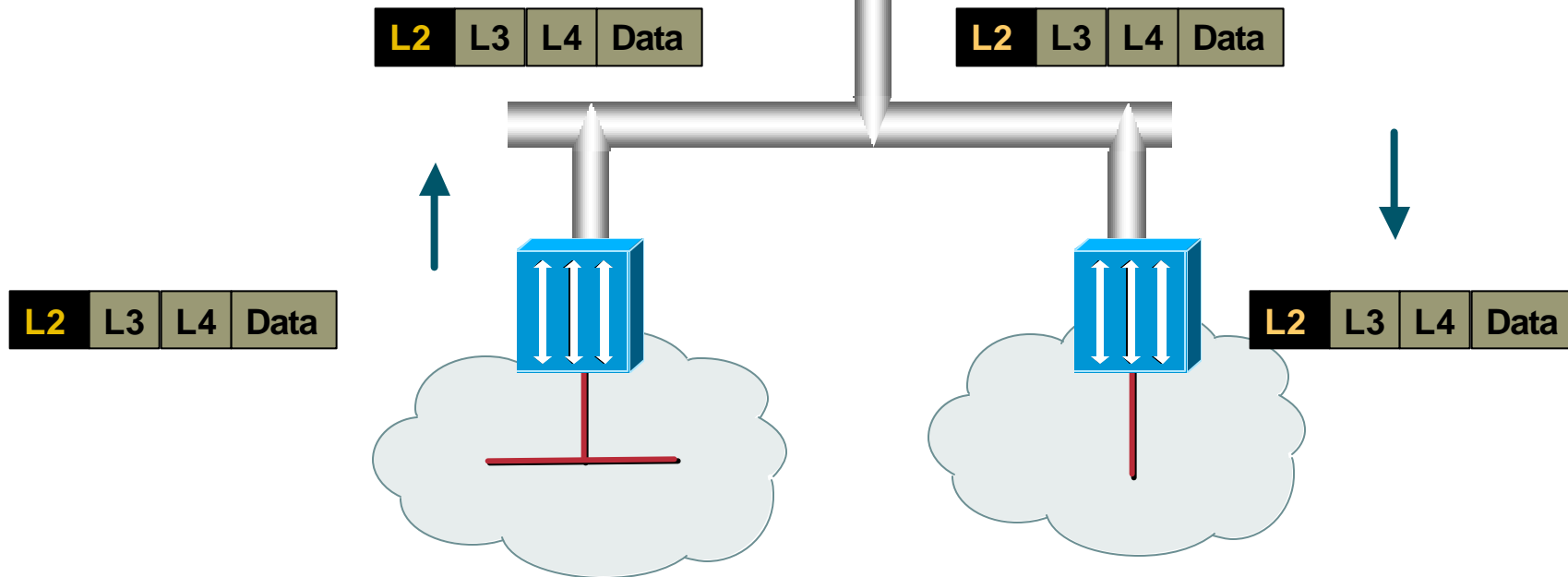


# Switching Table Construction

Frames enter the switch at ingress, and are stored in the shared memory buffer. The Destination MAC Address is mapped to the appropriate port number in the **Switching Table**.



Switching Table	
MAC Address	Port Number
00-10-A4-A6-FC-17	FastEthernet 0/14
00-10-B2-B4-FA-15	GigabitEthernet 0/1



# What Routers Really Do

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- **L3 classification**
- ***Forwarding Table* construction**
- ***Forwarding* decision making**
- **Other activities**

# Routers (Operationally)

- **Maintain/manipulate *Forwarding* information**
  - Listen for updates/update neighbors**
- **Classify packets for manipulation/queuing/permit-deny, etc.**
  - Compare packets to classification lists and perform control**
- **Perform Layer 3 switching**
  - Create outbound Layer 2 encapsulation**
  - Layer 3 checksum (IPv4 Only)**
  - TTL/hop count update**
- **Management/billing (statistics)**
  - Interface statistics—NetFlow export**
  - Telnet, SNMP, ping, trace route, HTTP**

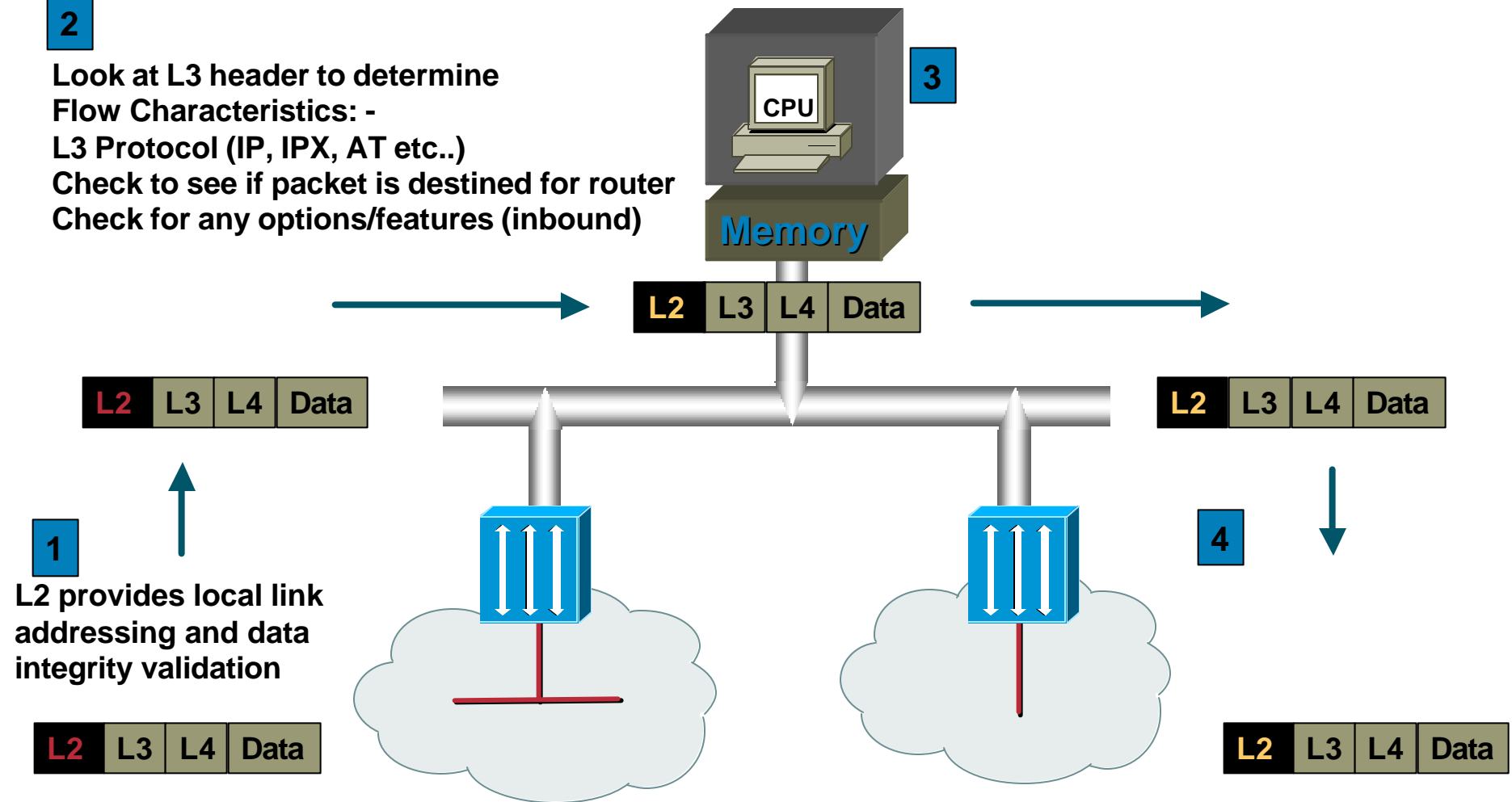
# Routers (Layer 3 Packet Functionally)

- **(Attempt to) switch packets**  
Layer 3 switching based on “*Forwarding*” information
- **(Attempt to) transmit packets**  
Access outbound memory (buffers) and media
- **Manipulate packets**  
Change contents of packet (CAR/NAT/compression/encryption)
- **Consume packets**  
Routing protocol updates etc.../services advertisements(SAP)/ICMP/SNMP
- **Generate packets**  
Routing protocol packets/SAPs/ICMP/SNMP  
Tunnels—GRE, IPSec, DLSw etc...

# L3 Classification

2

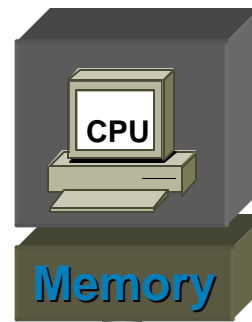
Look at L3 header to determine  
Flow Characteristics: -  
L3 Protocol (IP, IPX, AT etc..)  
Check to see if packet is destined for router  
Check for any options/features (inbound)



# Forwarding Table Construction

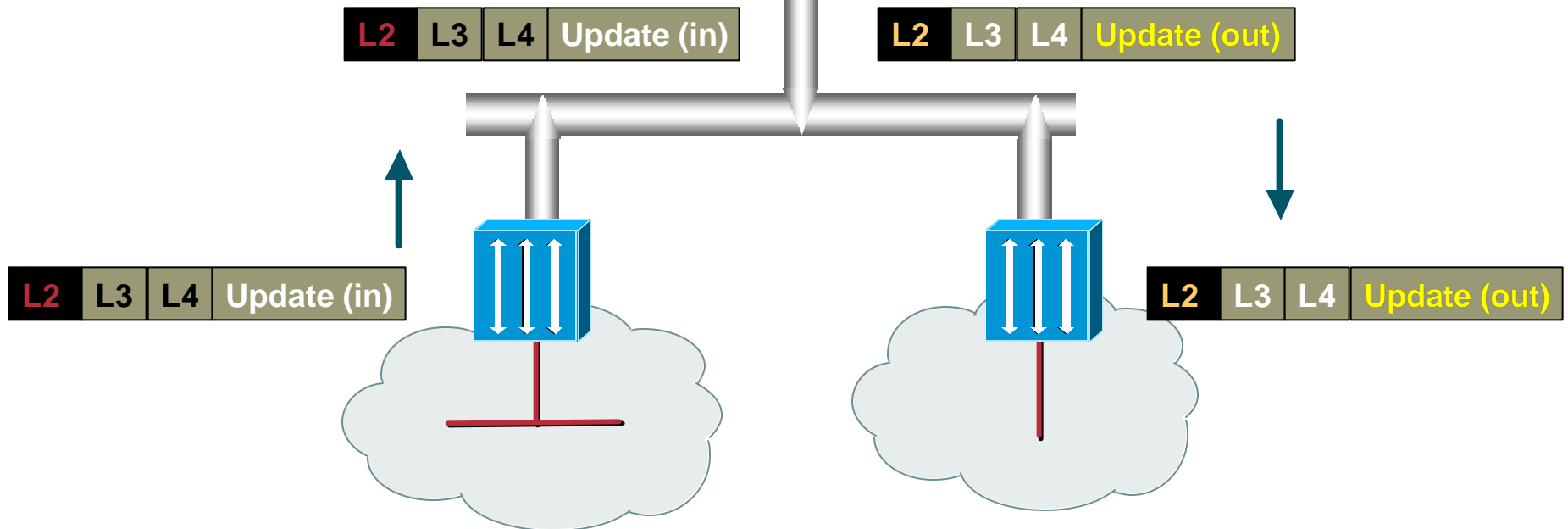
Update packets are queued for the CPU  
And dealt with by a appropriate software  
routine to build a **Forwarding Table**.

The router also looks at connected  
networks, Interface state and configured  
routes to complete the picture



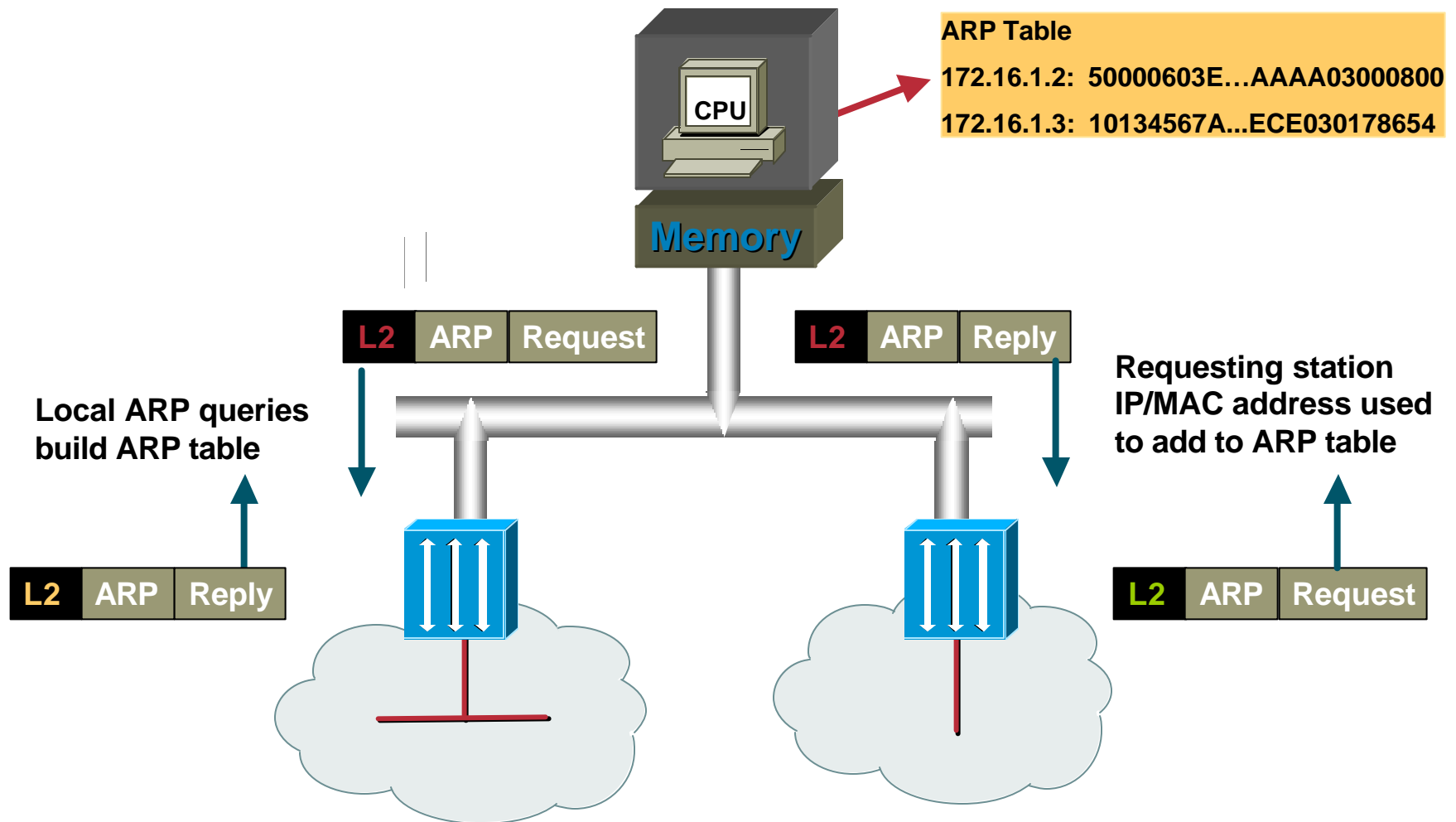
Forwarding Table	
172.16.2.0/24	via 172.16.1.2
10.1.1.0/24	via 172.16.1.2

Updates are generated by the router and  
queued for transmission on interfaces  
configured for the given protocol



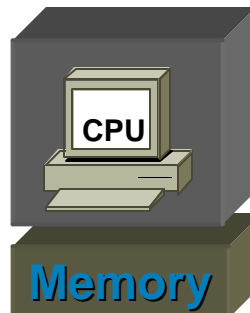
# Forwarding Table Construction

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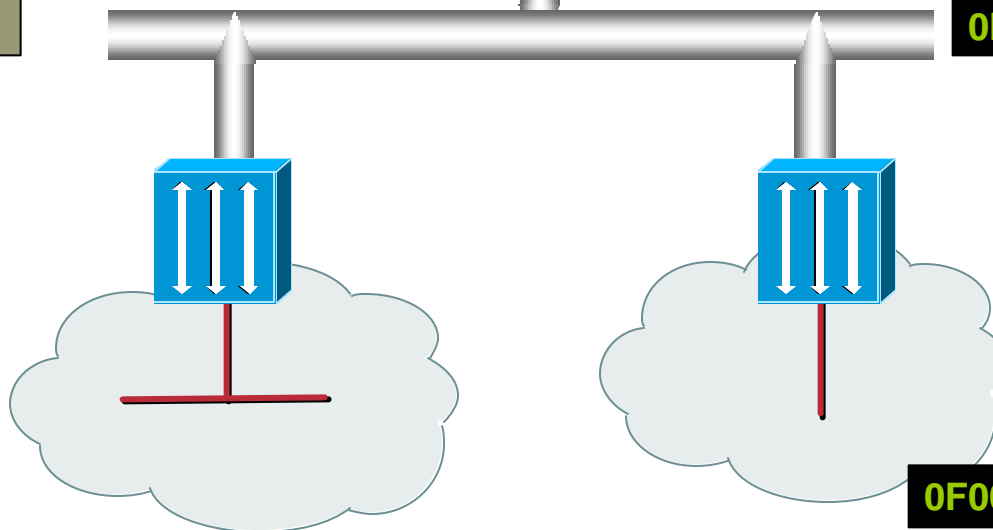
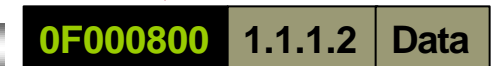
# L3 Forward to Next Hop

Look at L3 header to determine Flow Characteristics: -  
 L3 Protocol (IP, IPX, AT etc..)  
 Check to see if packet is destined for router  
 Check for any options/features (inbound)



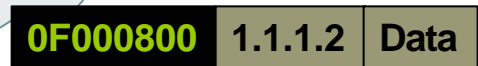
Forwarding Table	
1.1.0.0/16	via 172.16.2.1
10.1.1.0/24	via 172.16.1.1

ARP Table	
172.16.2.1:	0F000800
172.16.1.1:	10134567A...ECE030178654



L2 is just used for local link addressing and data integrity validation

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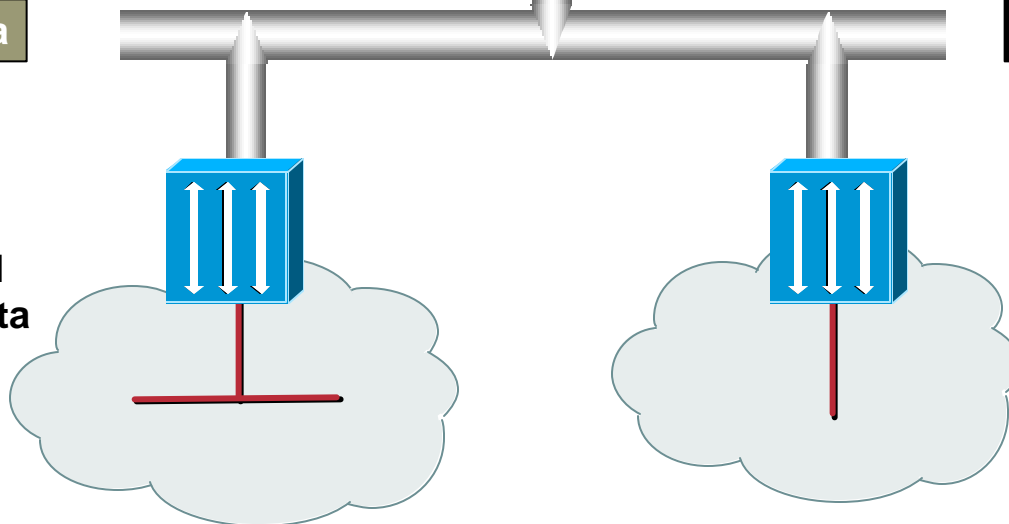
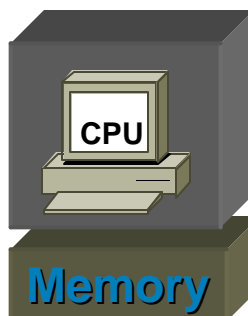


Destination

# Other Activities

Check IP header Checksum (IPv4)  
Check TTL  
Check for ability to Fragment  
Check packet against various feature lists  
(I/P ACL's, NAT, CAR, RFP etc)

Decrement TTL  
Re-write IP header Checksum (IPv4)  
Fragment  
Check packet against various feature lists  
(O/P ACL's, NAT, Queuing)

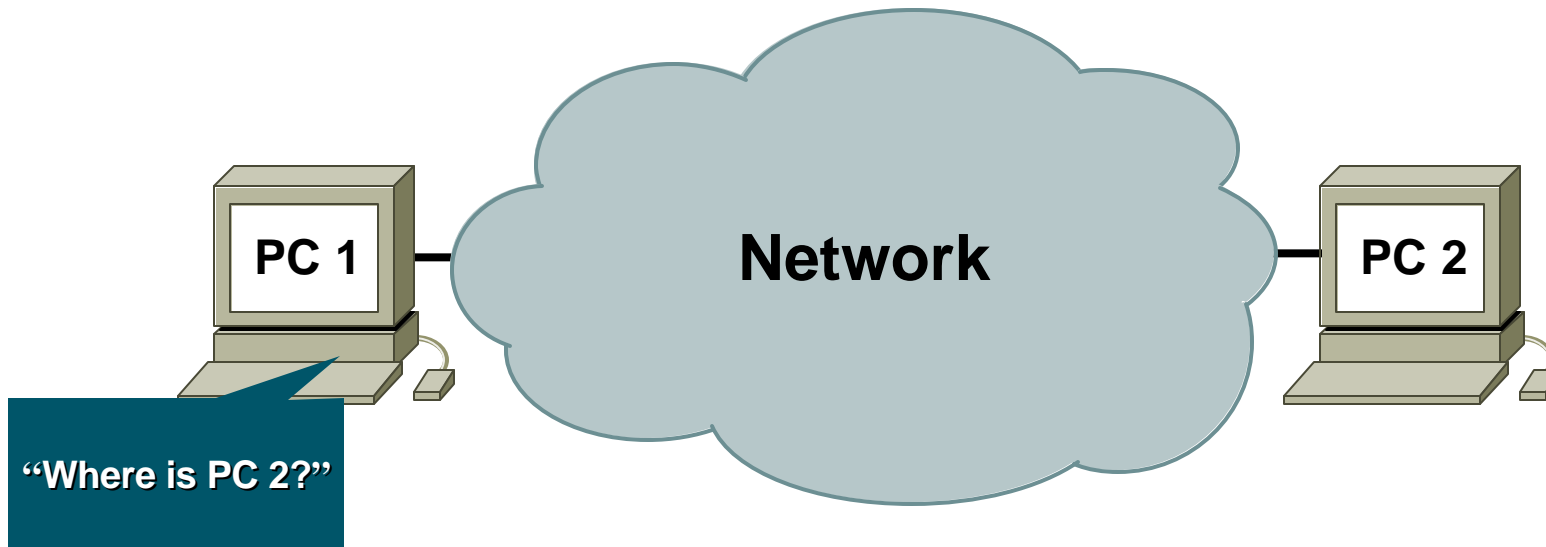


L2 is just used for local link addressing and data integrity validation

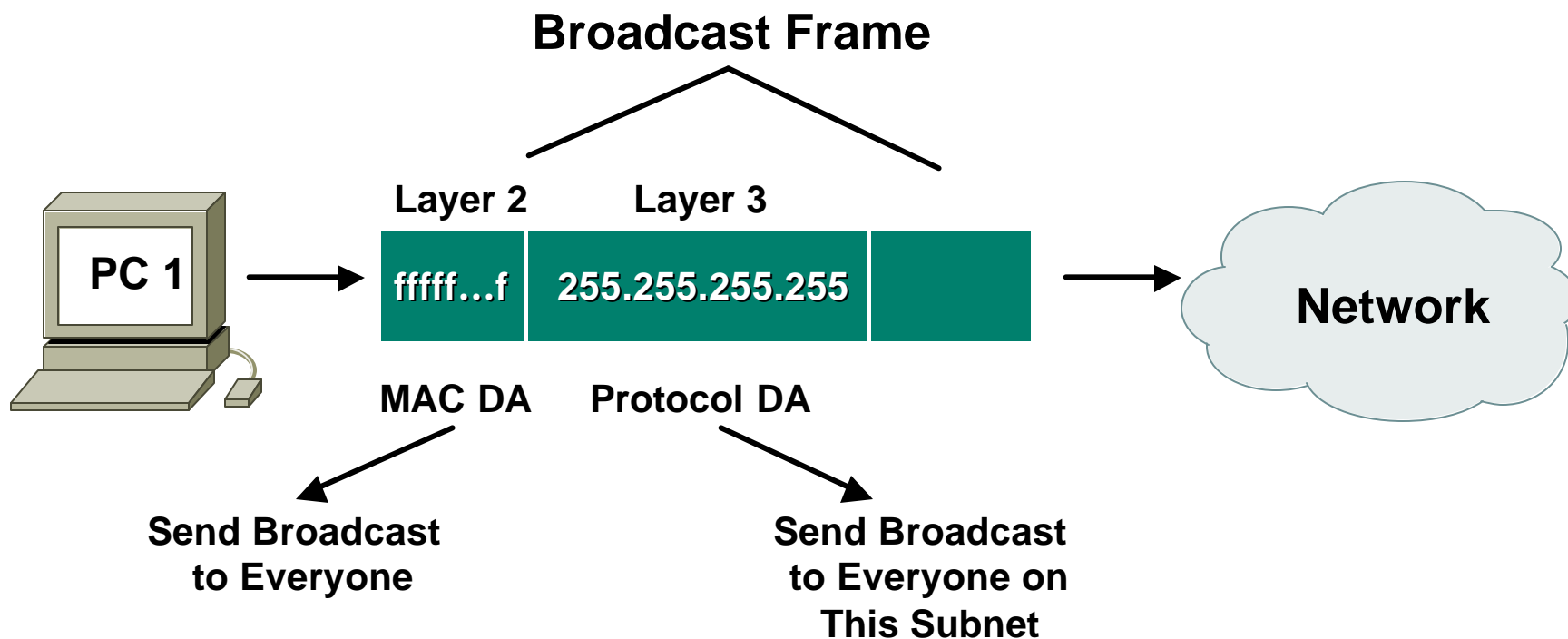
L2 is just used for local link addressing and data integrity validation



# How Do I Find PC 2?



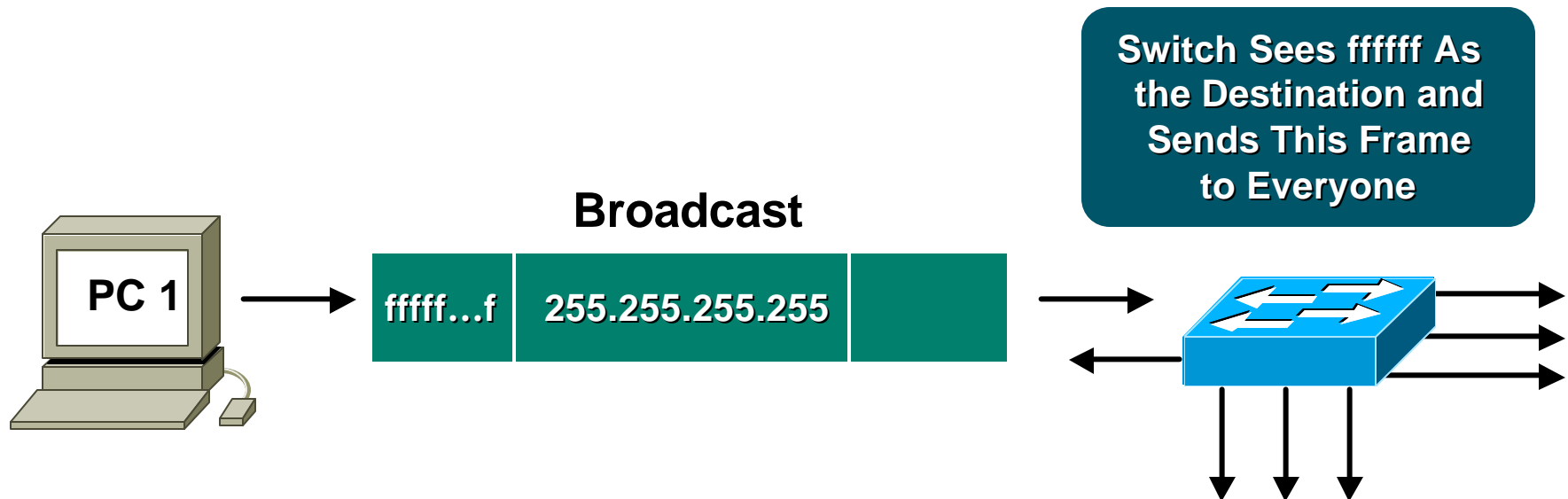
# Broadcast?



**PC 1 Sends a Broadcast to See If PC 2 Is Locally Connected**

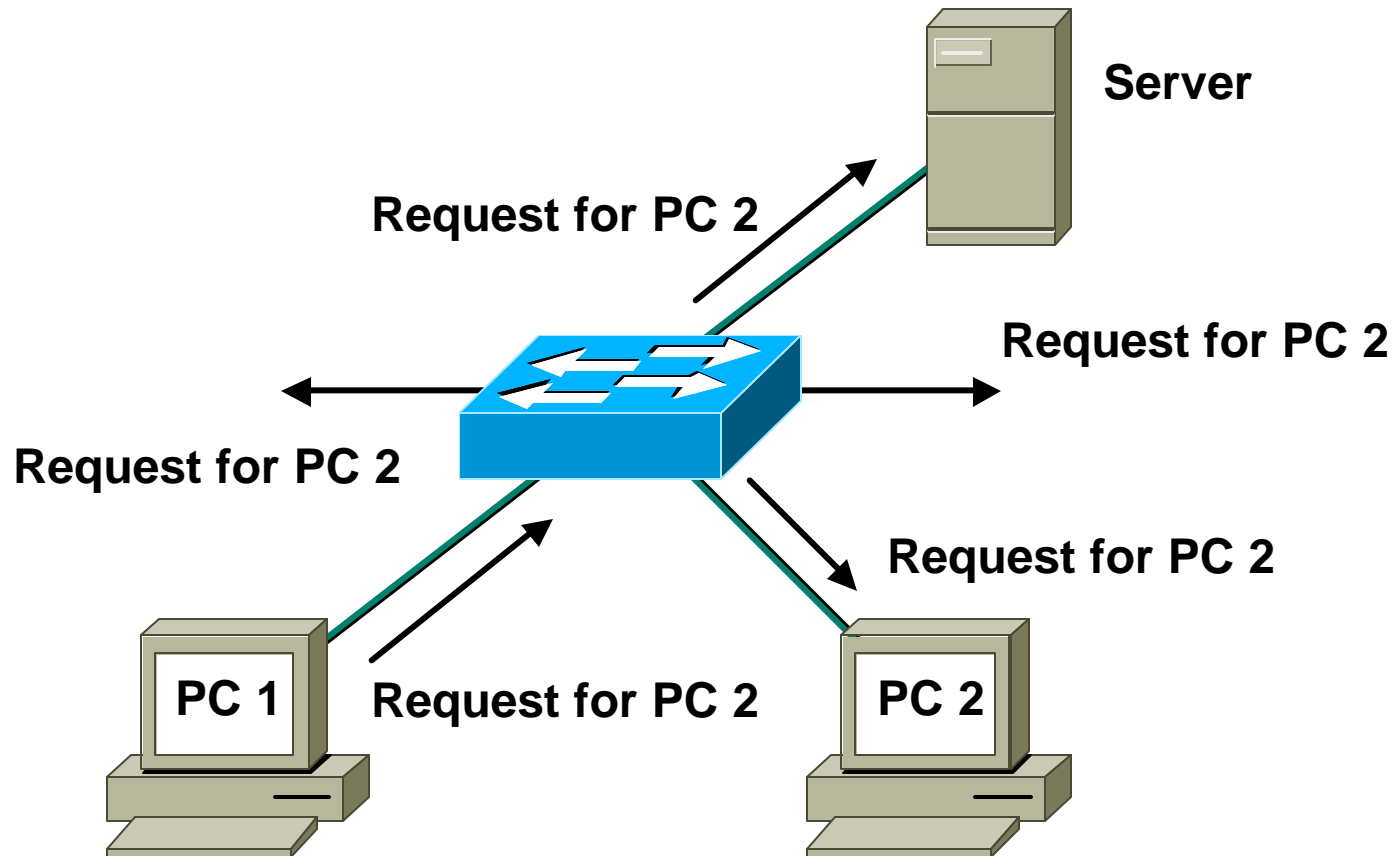
# Broadcast Propagation—L2 Switch

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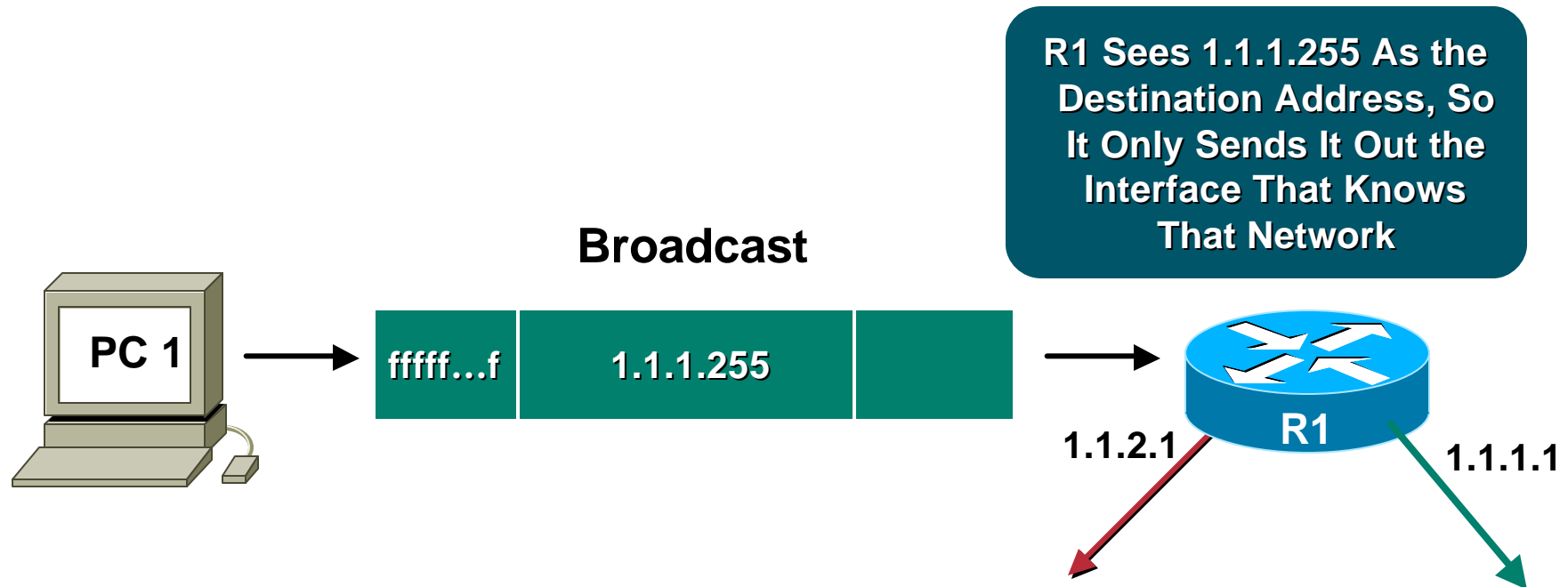
- **Switch sends the broadcast frame out all the ports within the broadcast domain**

# Broadcast L2 Example



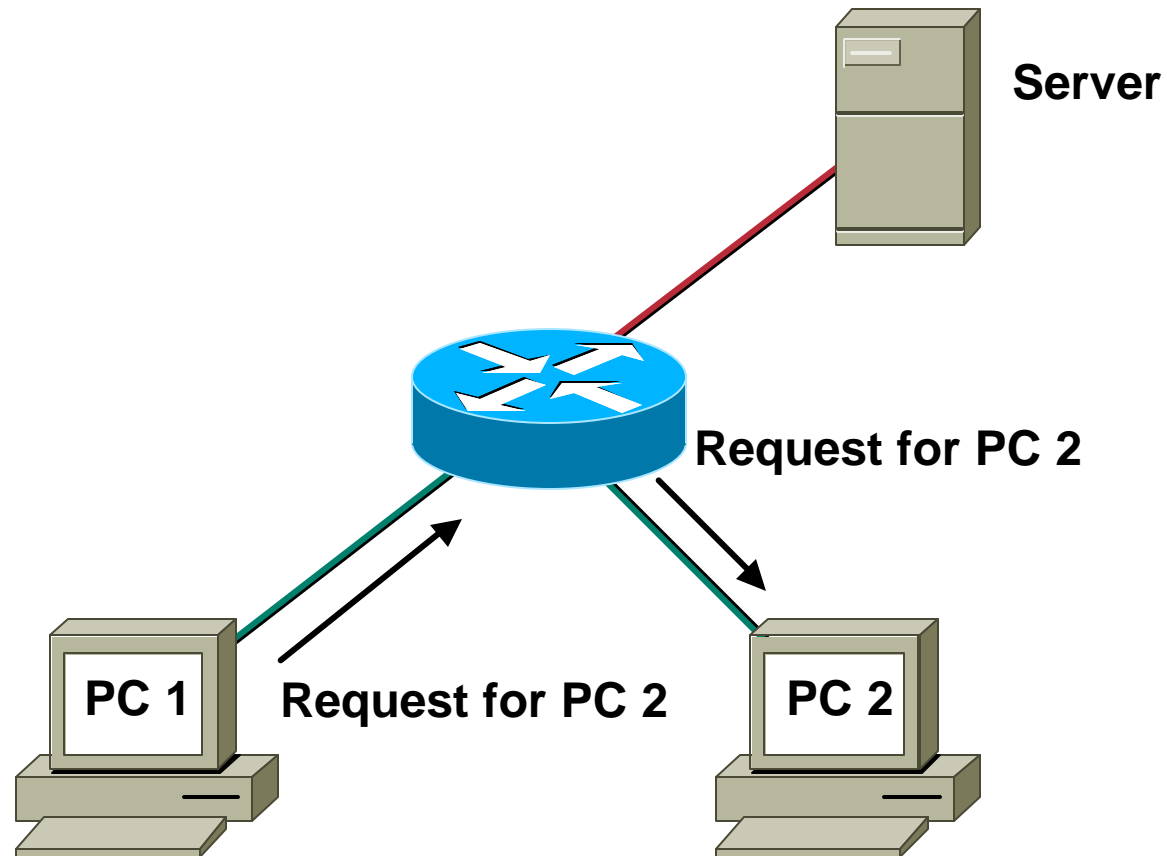
# Broadcast Propagation—L3 Routing

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- Router terminates the broadcasts, does not propagate them everywhere

# Broadcast L3 Example



# Components of an Architecture

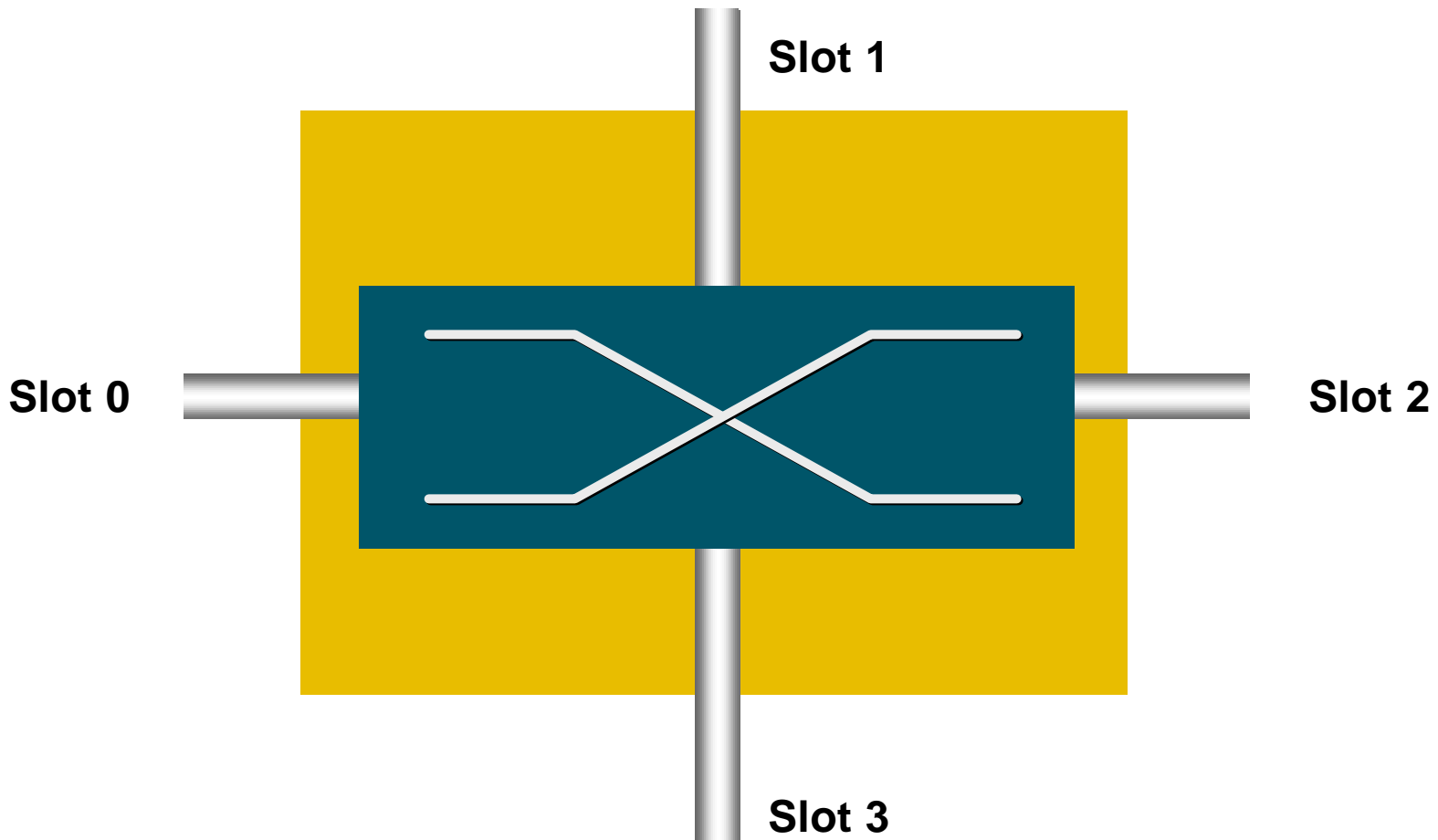
# Components of an Architecture

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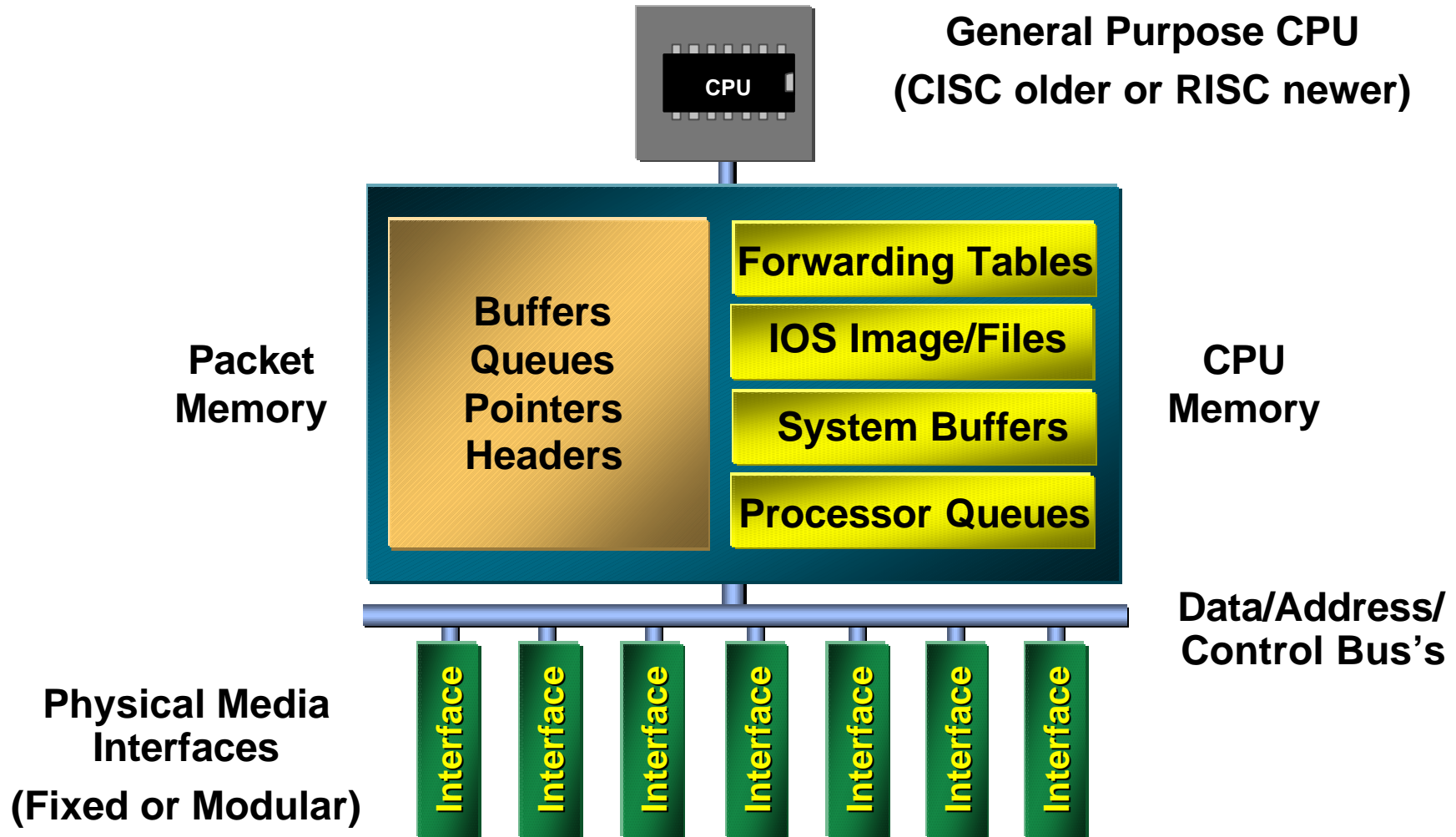
- **Switching fabric**
- **Memory/buffers**
- **Queuing**
- **Distributed vs. centralized**
- **Forwarding architectures**

# Switching Fabric

## Connection Between the Slots/Ports in a Switch



# Shared Memory

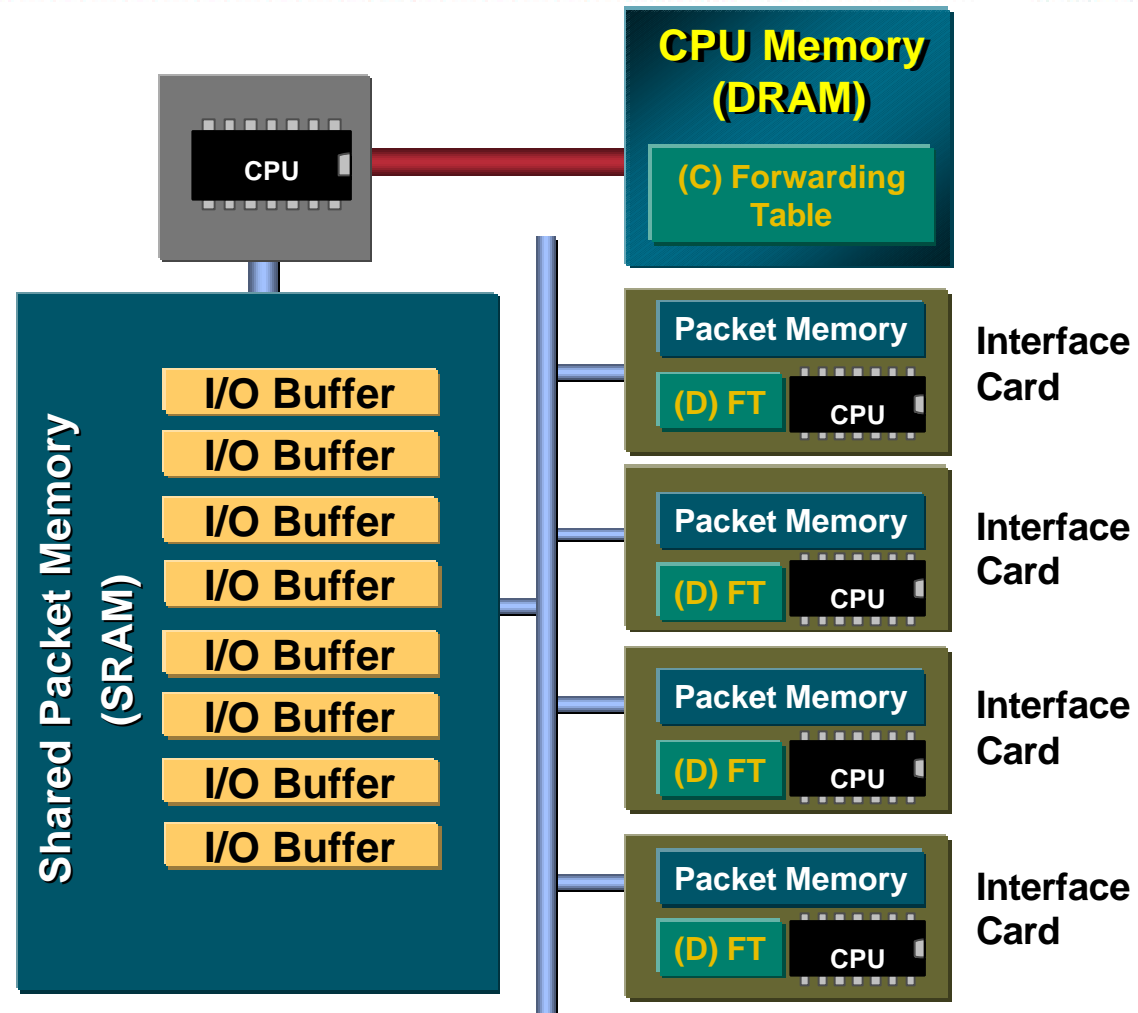


# Shared Memory (Distributed Processors/Memory)

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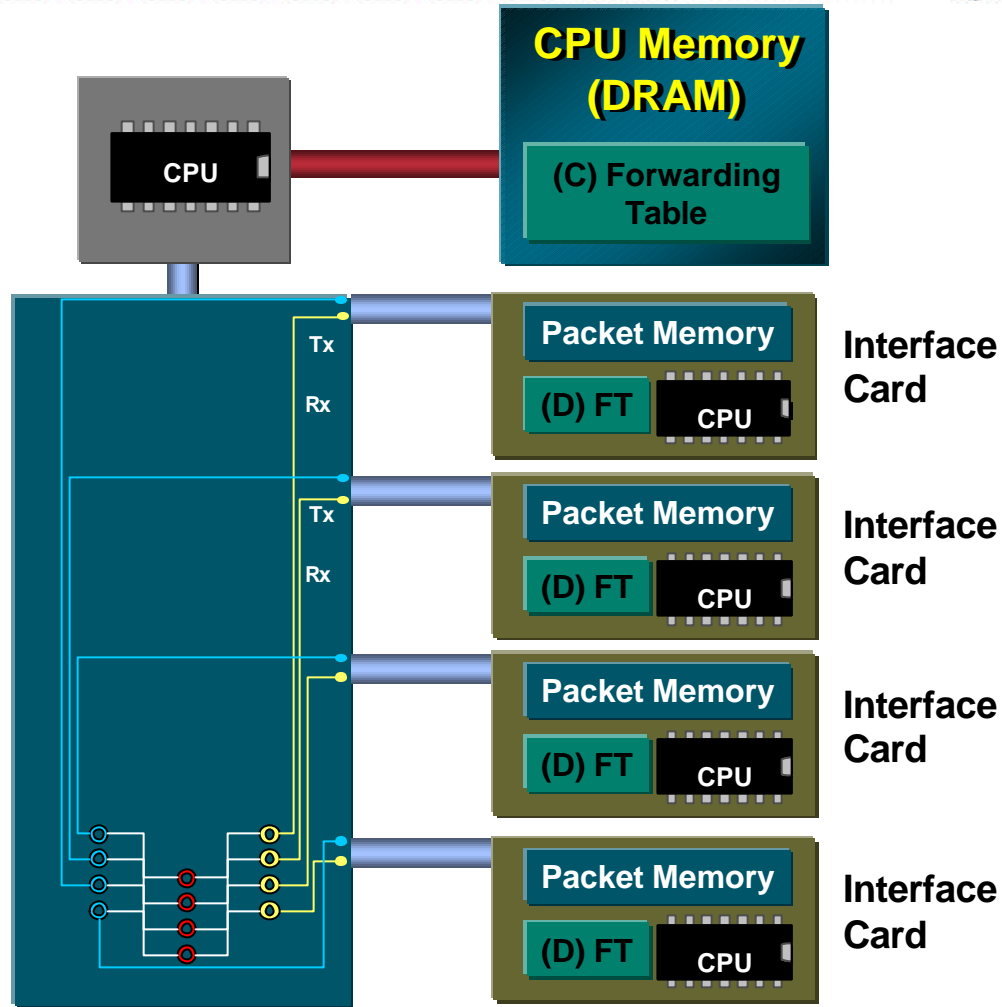
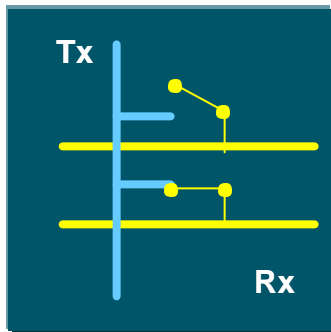
Each Line card has Packet Memory, Forwarding Table Memory and a discrete CPU.

A Copy of the central forwarding table is propagated from the Central Route Processor to the Line Cards for Local switching of packets



# Cross Bar Data Path

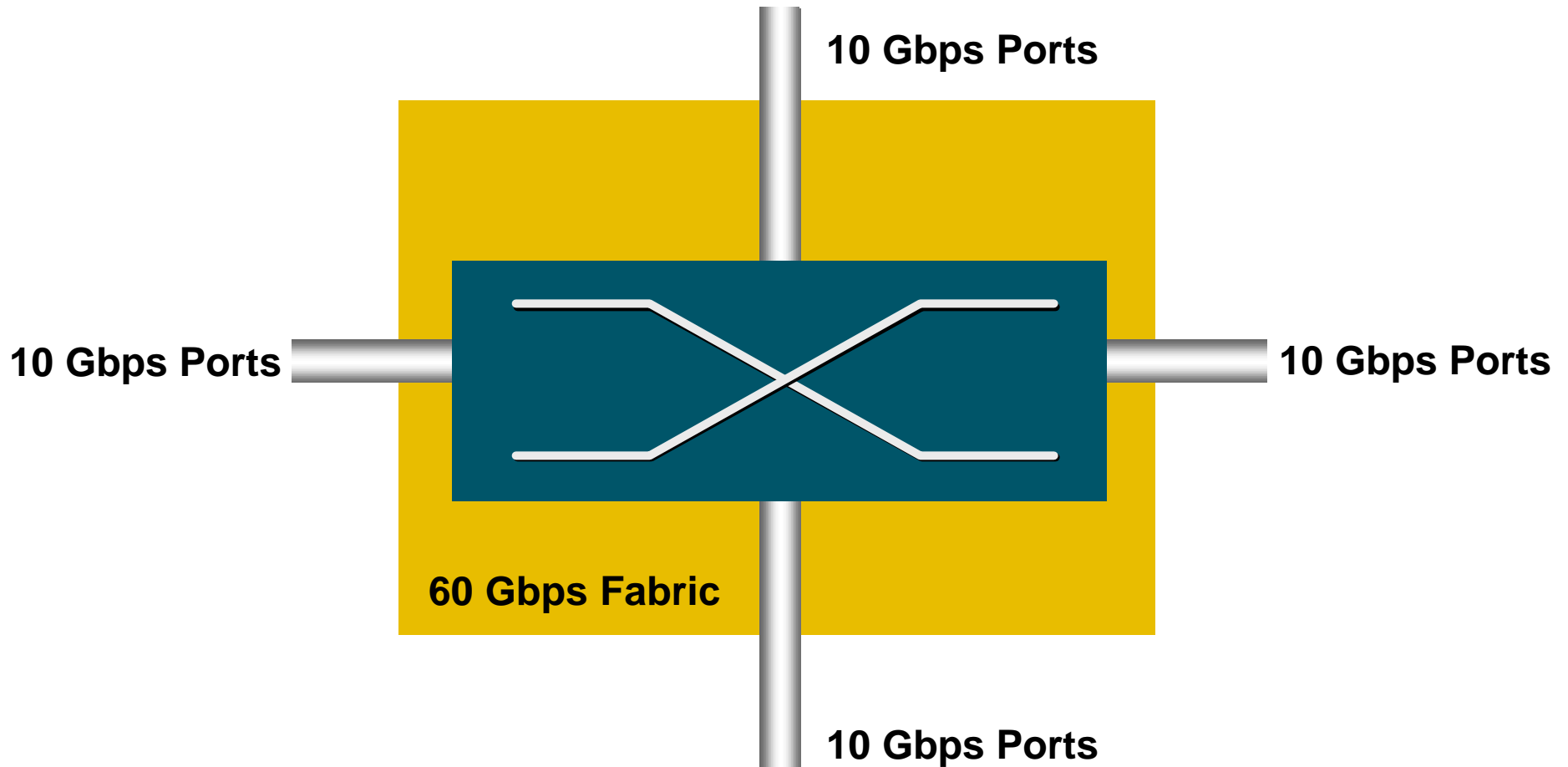
- Multiple conflict free paths
- Typically higher bandwidth capacity
- Signaling and Scheduling more complex



ASIC X-Bar Fabric

# Non-Blocking Switching Fabric

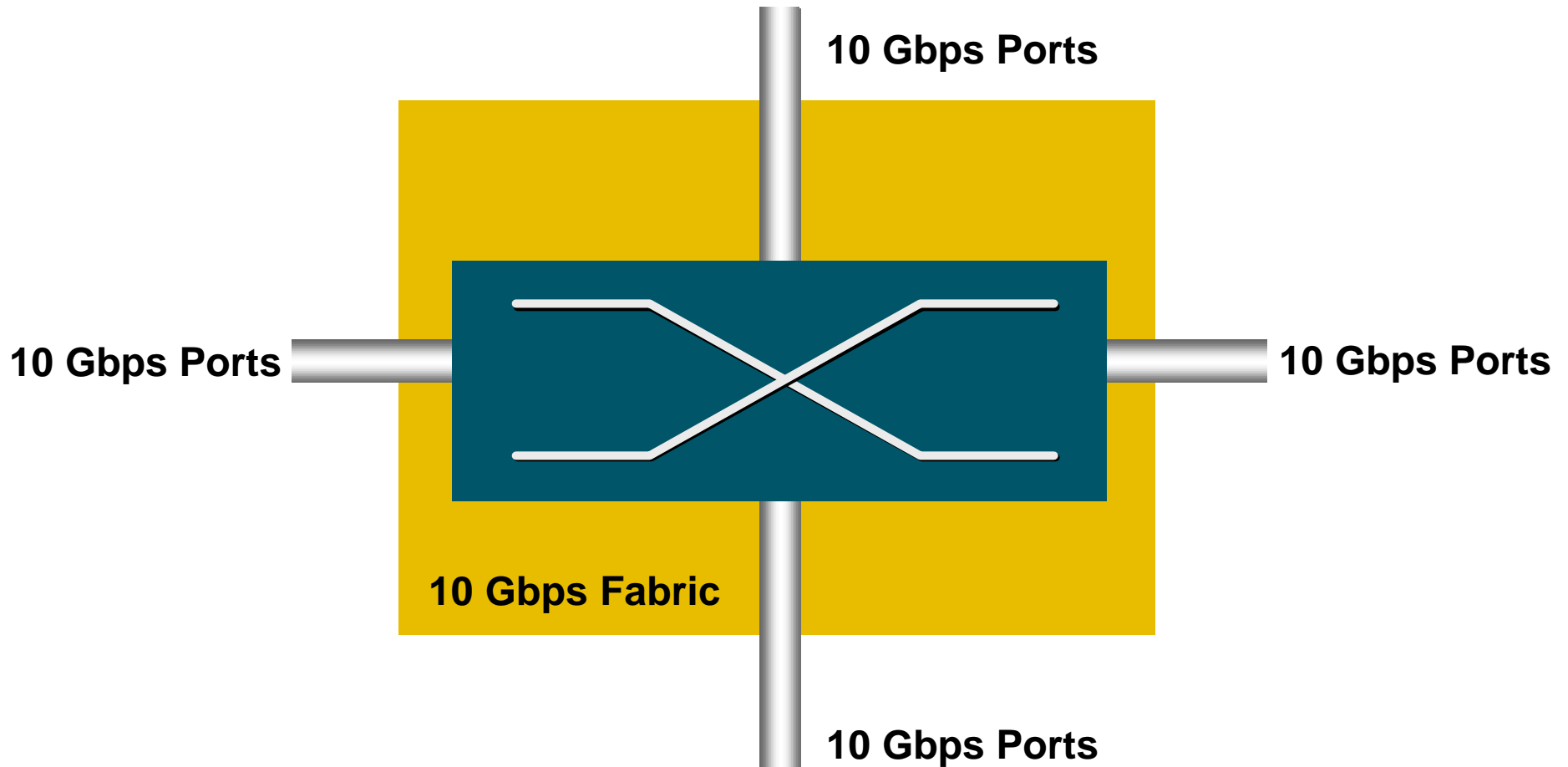
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**Speed of Fabric > Ingress + Egress**

# Blocking Switching Fabric

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**Speed of Fabric < Ingress + Egress**

# Components of an Architecture

- **Switching fabric**
- **Memory/buffers**
- **Queuing**
- **Distributed vs. centralized**
- **Forwarding architectures**

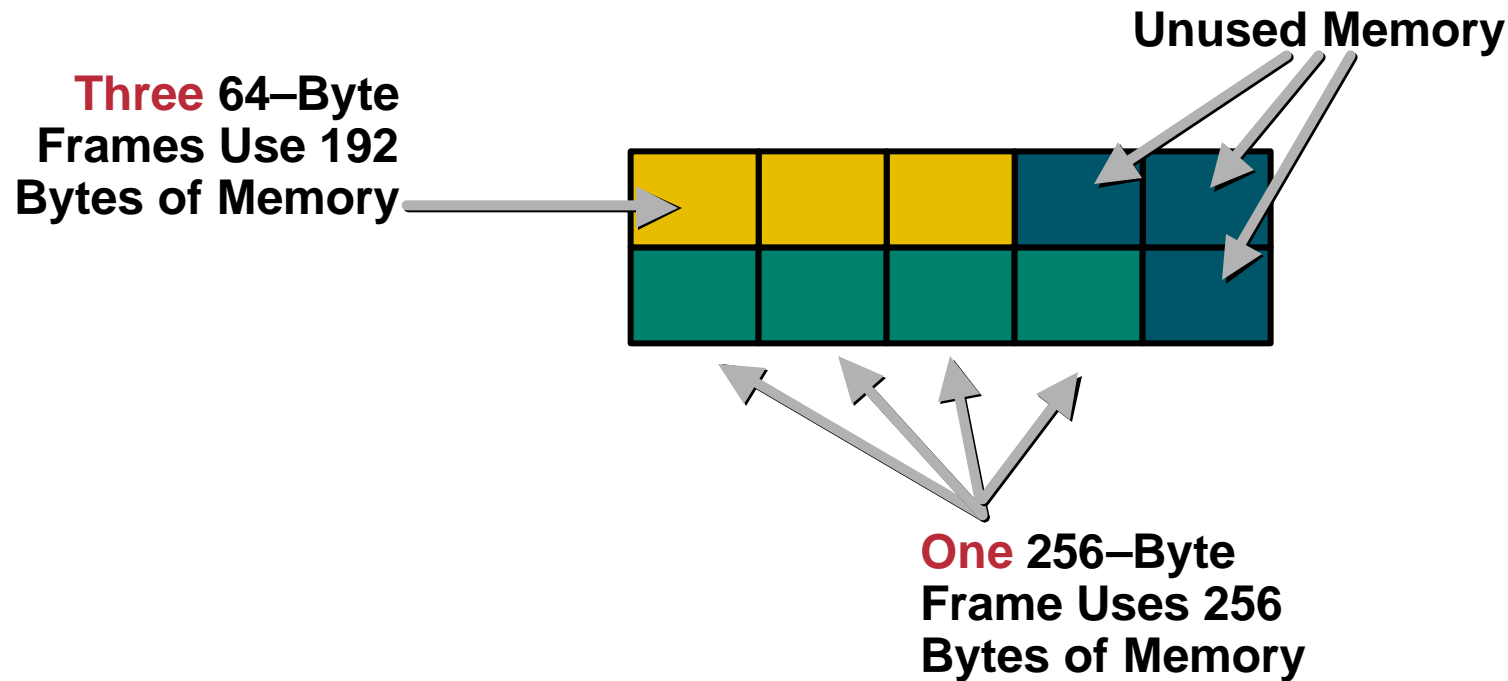
# Contiguous Buffer Allocation

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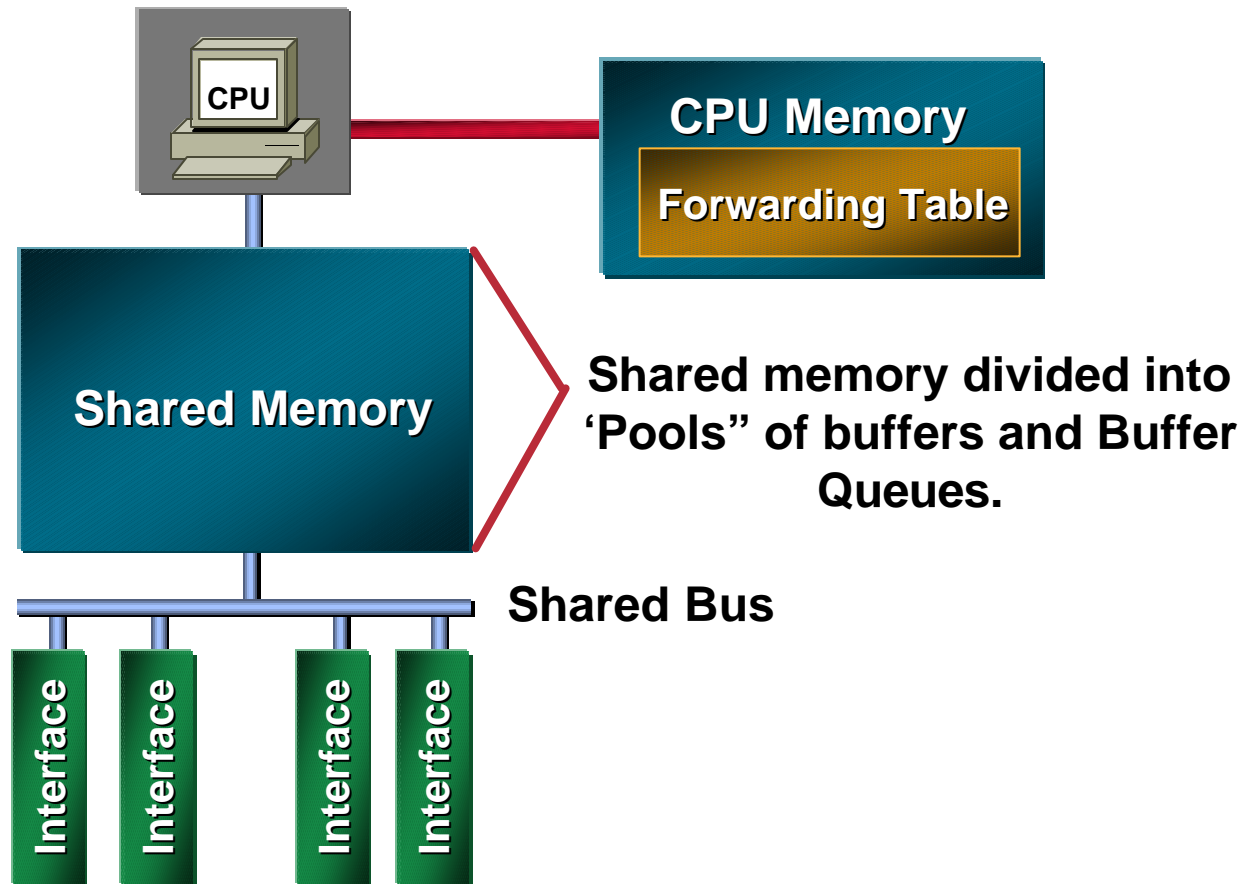
- Buffer length fixed in size (often to MTU)
- Less expensive than particle buffering architectures
- Inefficient use of buffers

# Particle Buffer Allocation

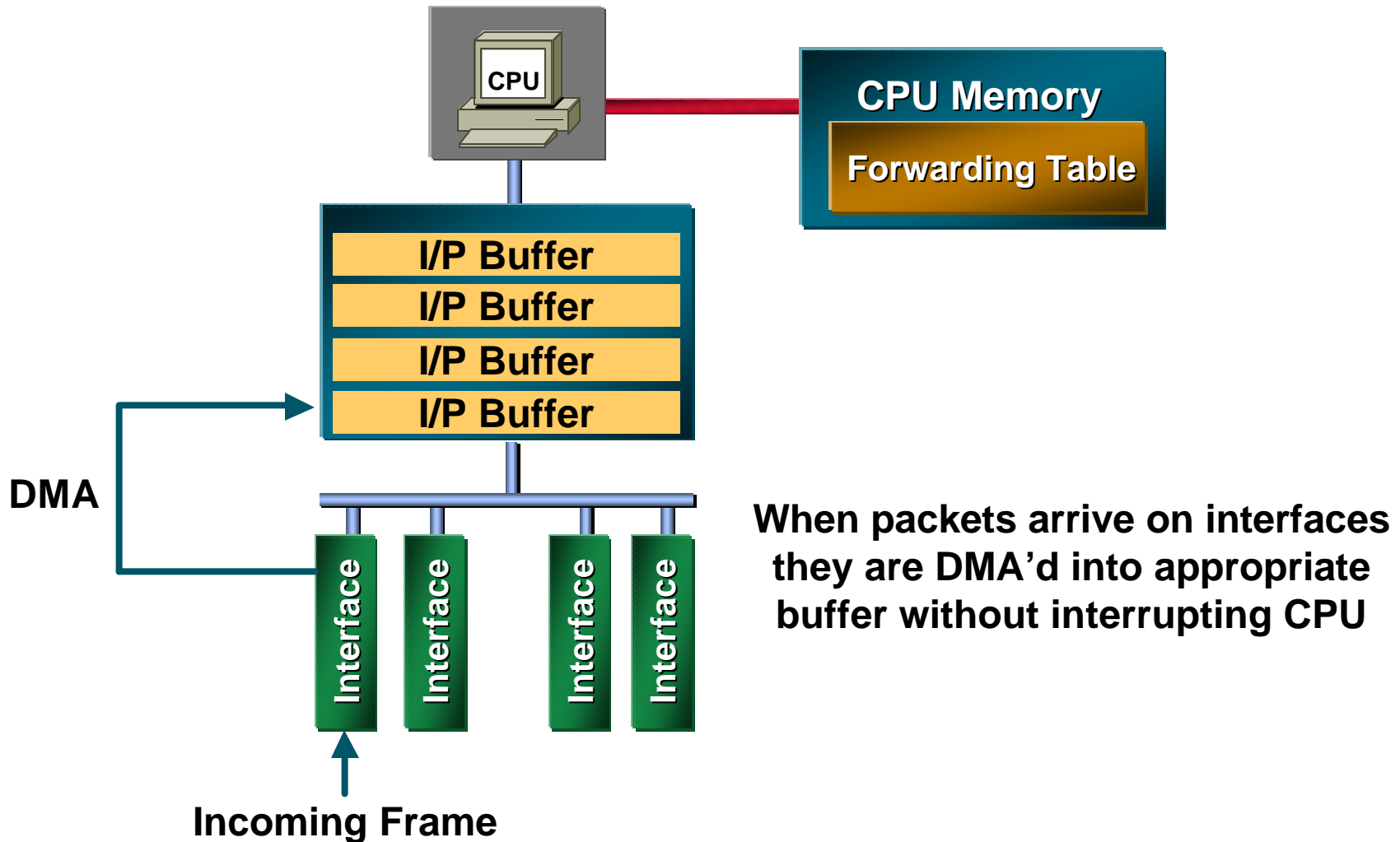


- Each buffer fixed in small increments (for example, 64 bytes each)
- Allows for efficient use of buffers

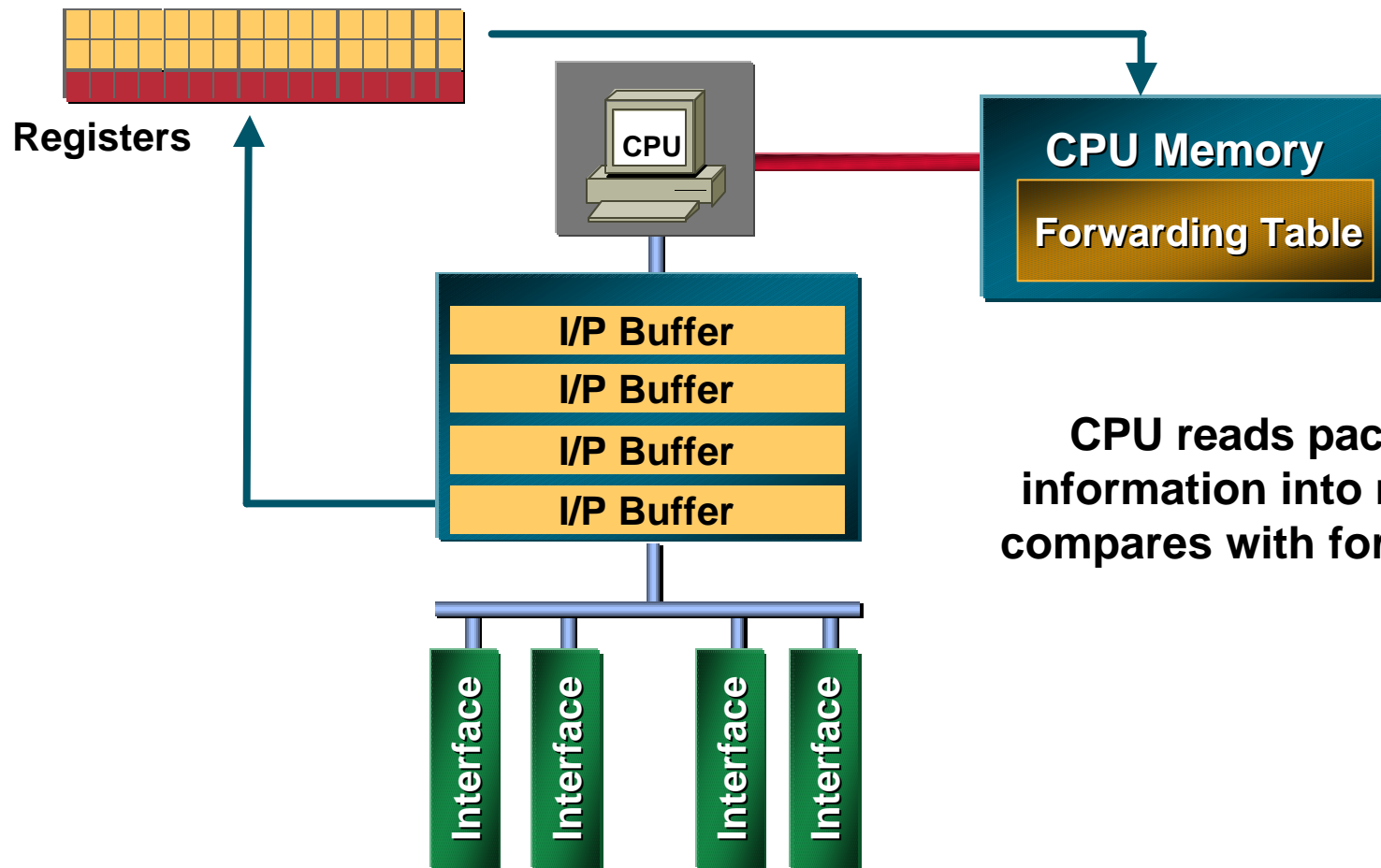
# Shared Memory



# Shared Memory



# Shared Memory



**CPU reads packet header information into registers and compares with forwarding table**

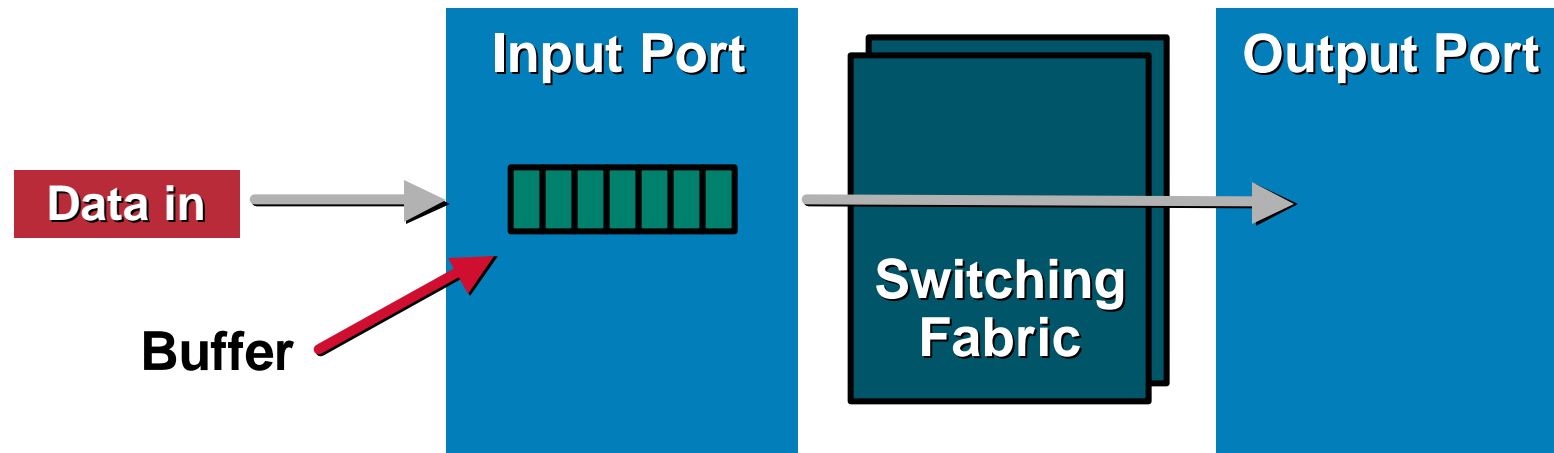


# Components of an Architecture

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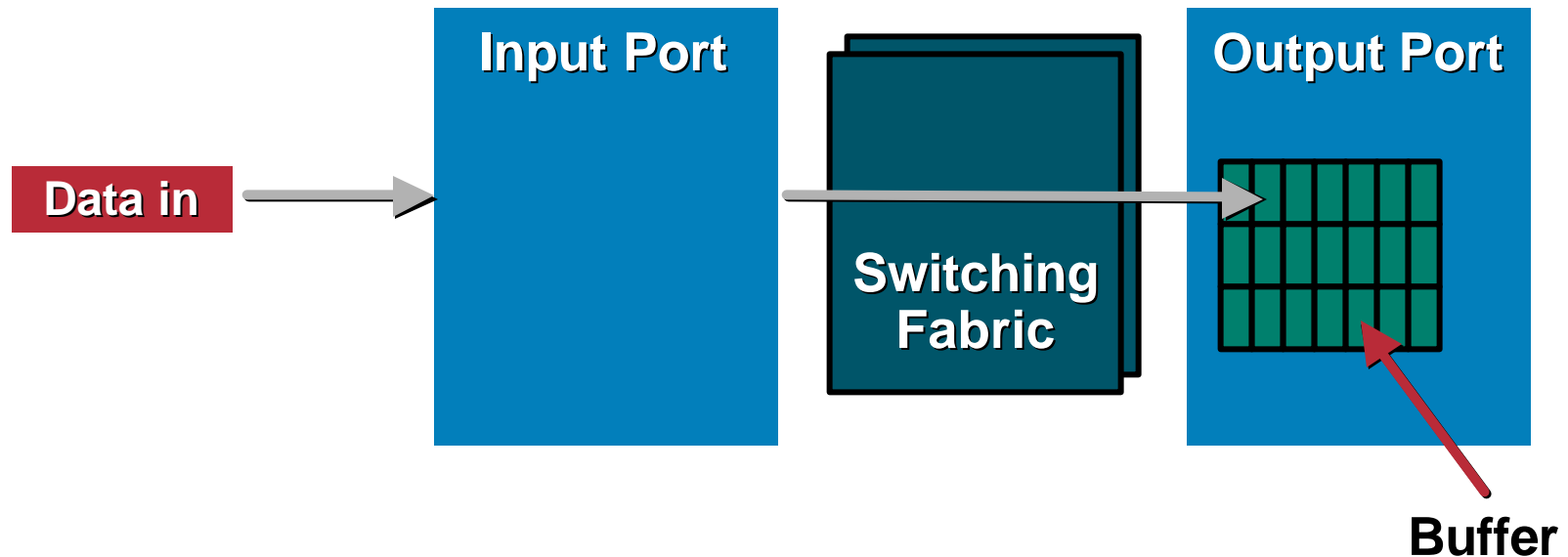
- **Switching fabric**
- **Memory/buffers**
- **Queuing**
- **Distributed vs. centralized**
- **Forwarding architectures**

# Input Queuing



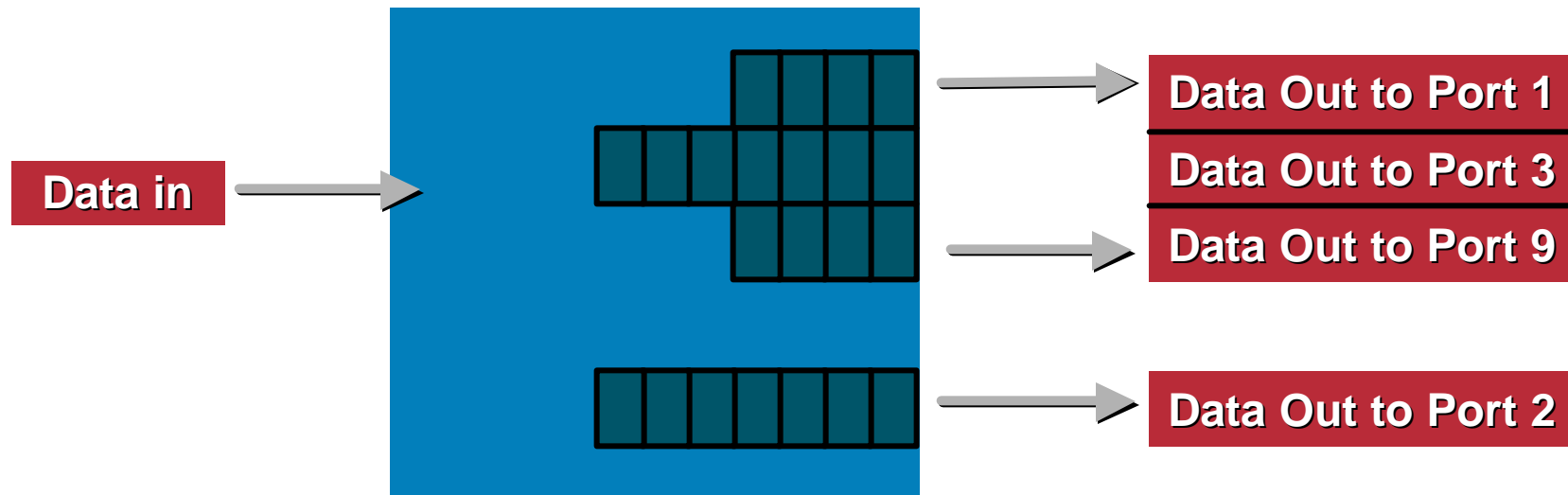
- Packets buffered at the inbound port
- Can result in head of line blocking if you have a single input queue per port
- Can reduce throughput

# Output Queuing



- **Buffers at the output port**
- **Allows for individual prioritization of traffic flows**

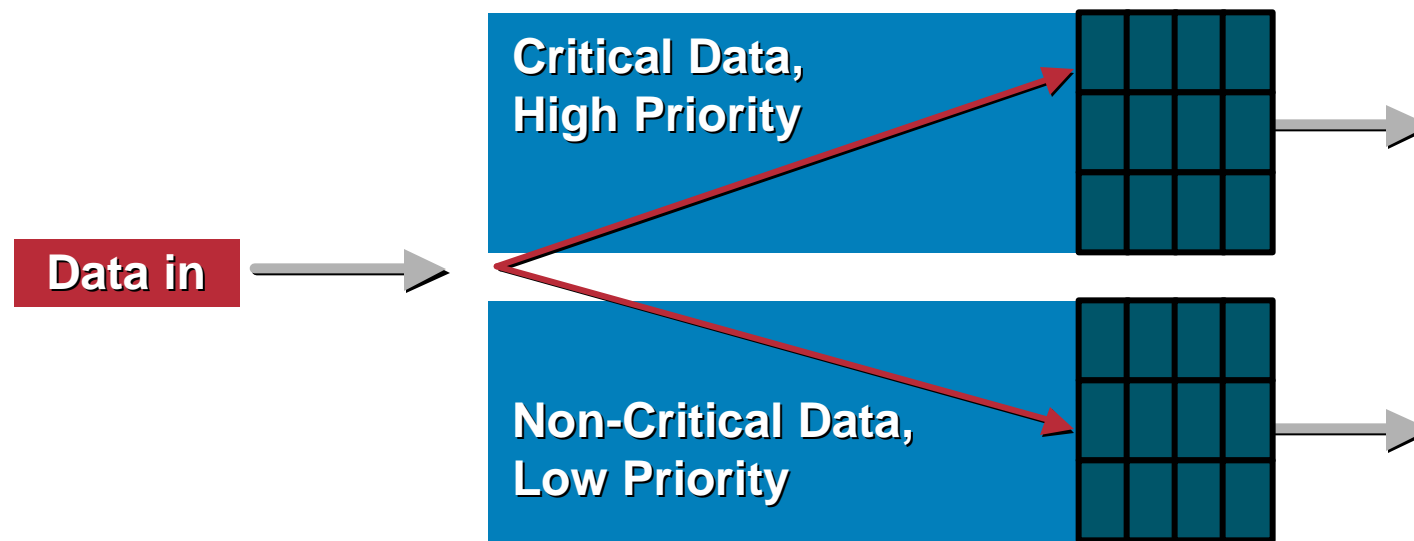
# Output Queuing/Shared Buffer



- **Central pool of buffers shared between all ports**
- **Maximum throughput with fewest buffers**
- **No head of line blocking with intelligent congestion management**

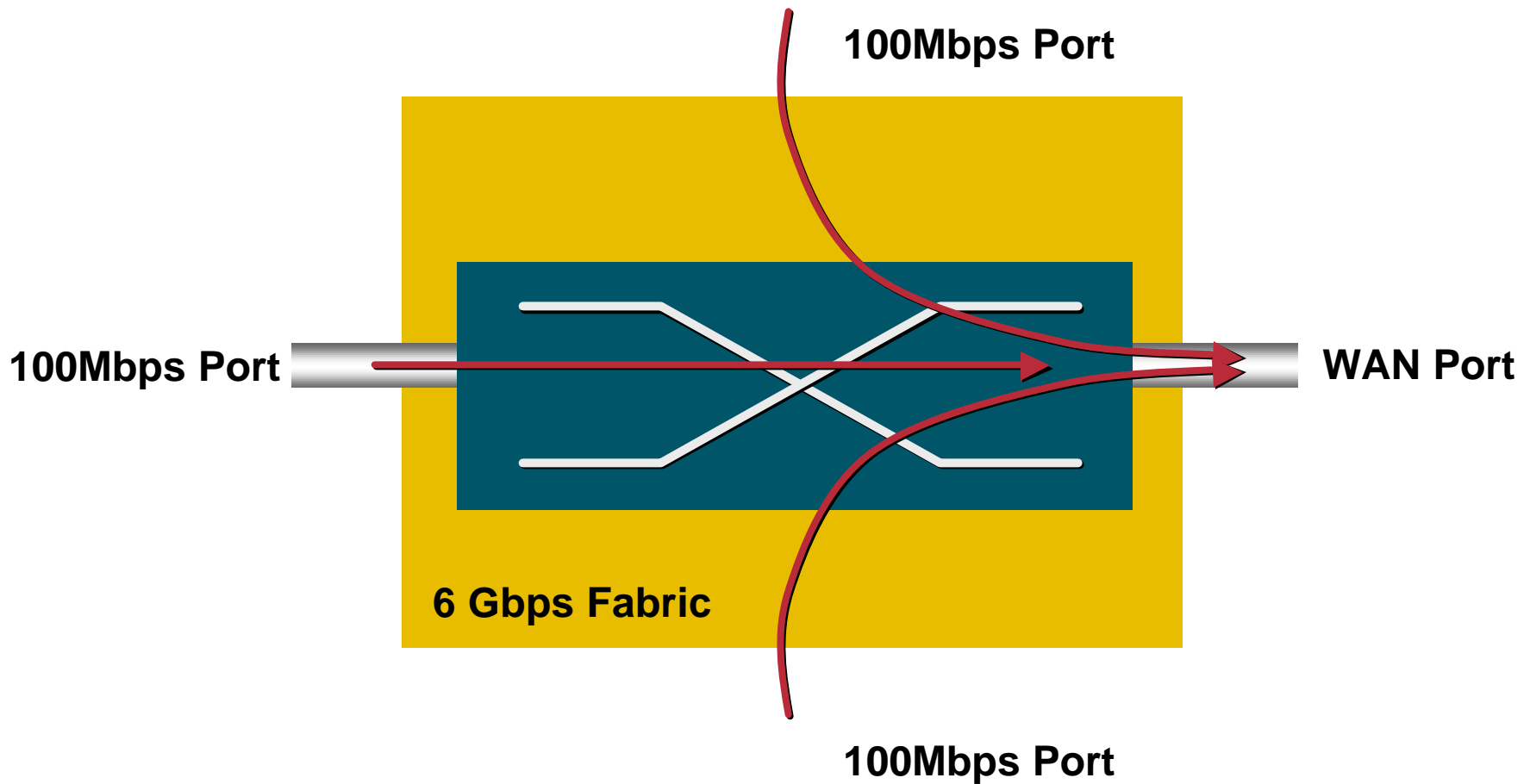
# Multiple Queues Per Port

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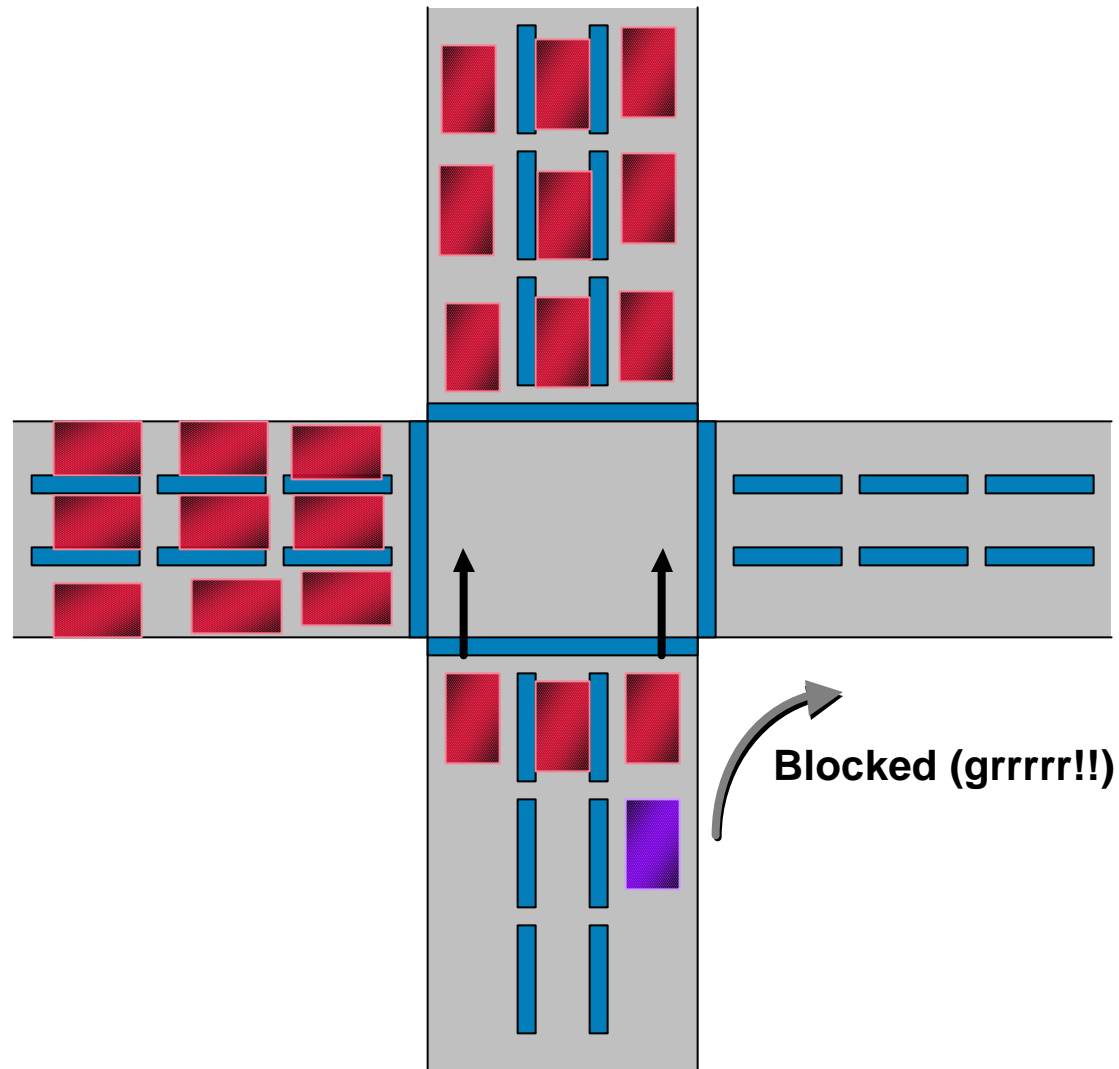


- Can be implemented in either output queuing or shared memory models
- Scheduling and/or congestion avoidance algorithm required
- **Note: Number of queues affect overall number of buffers per queue**

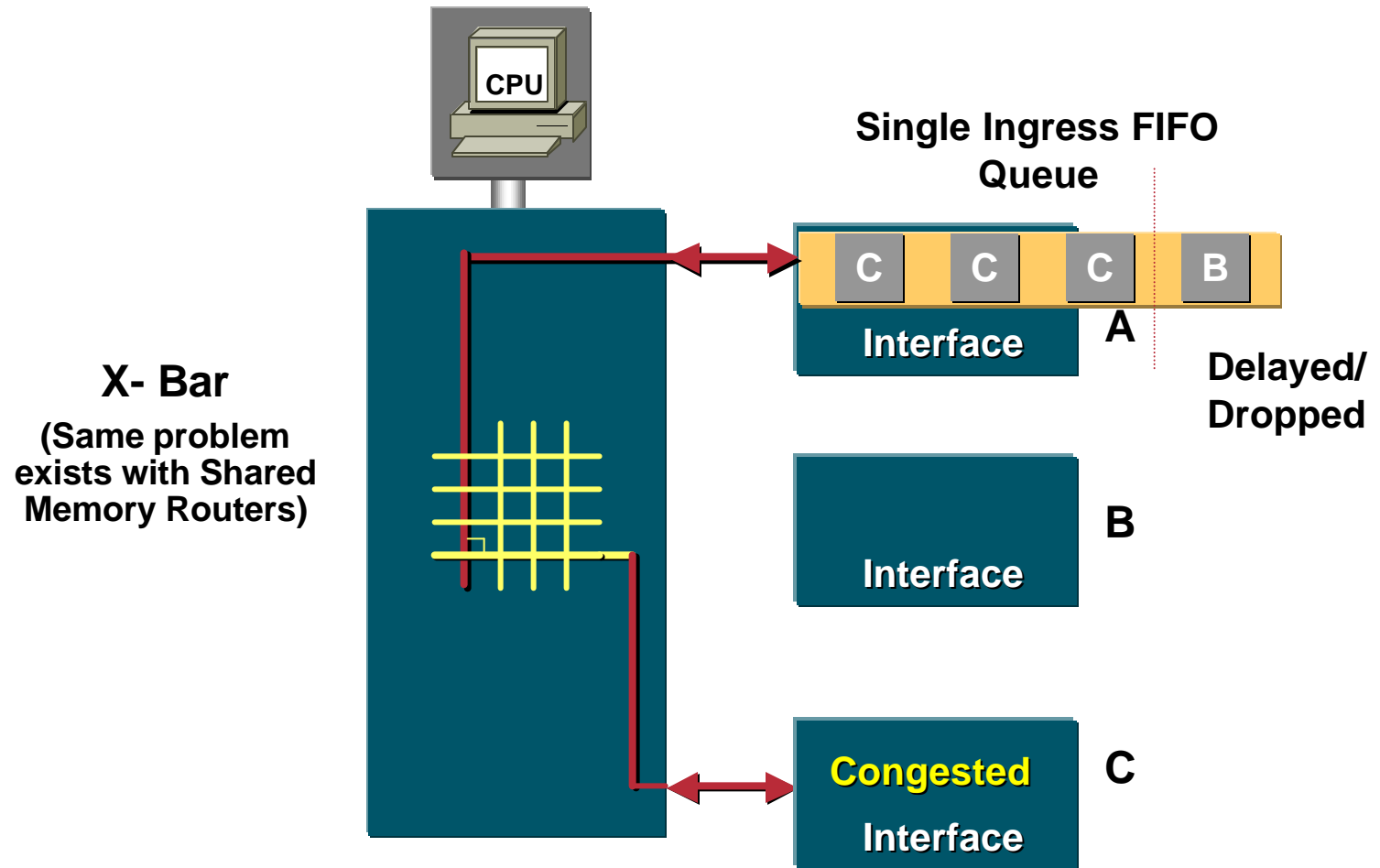
# How Does Traffic Run in a Real Network?



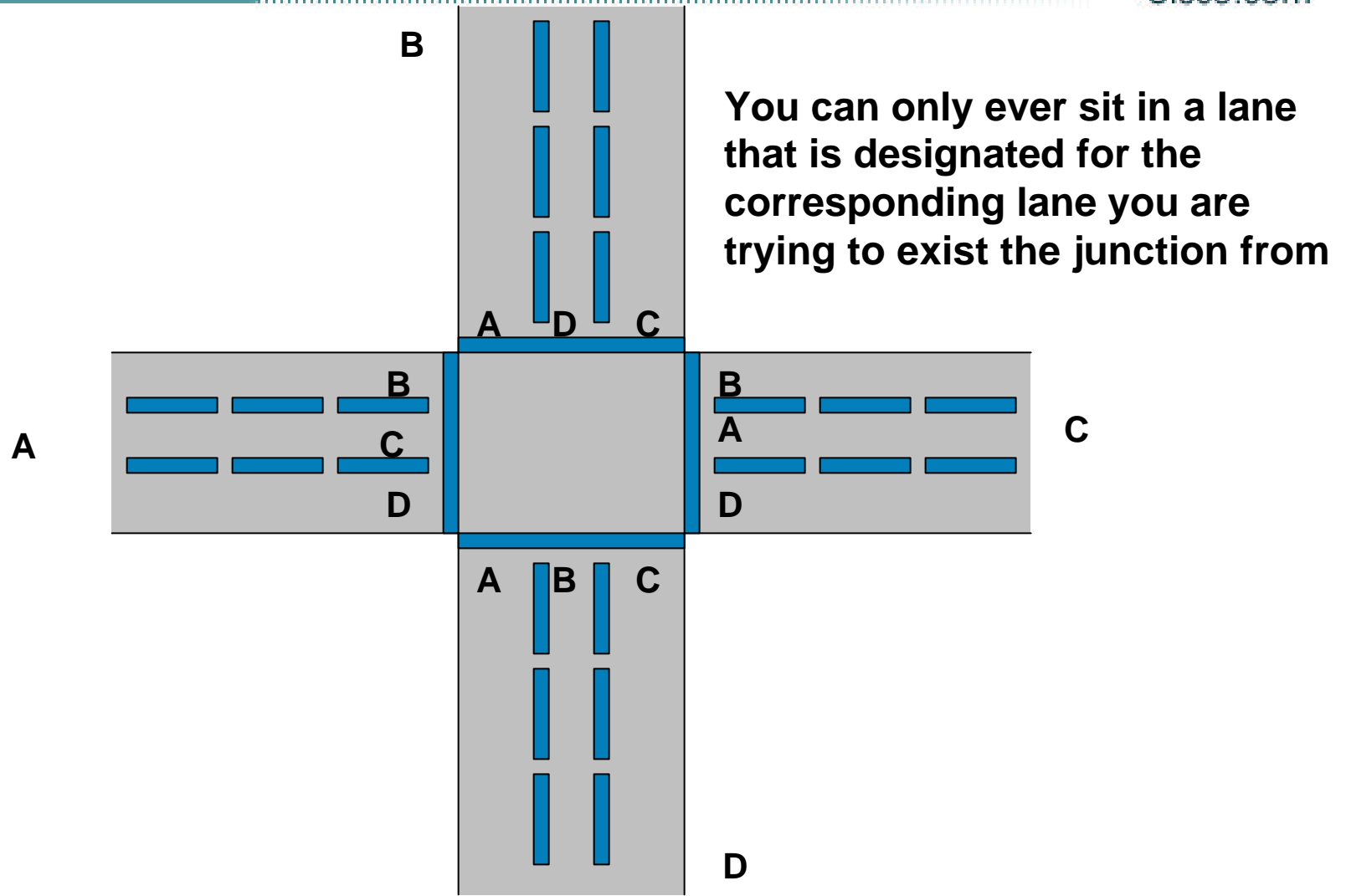
# Head of Line Blocking (HOL)



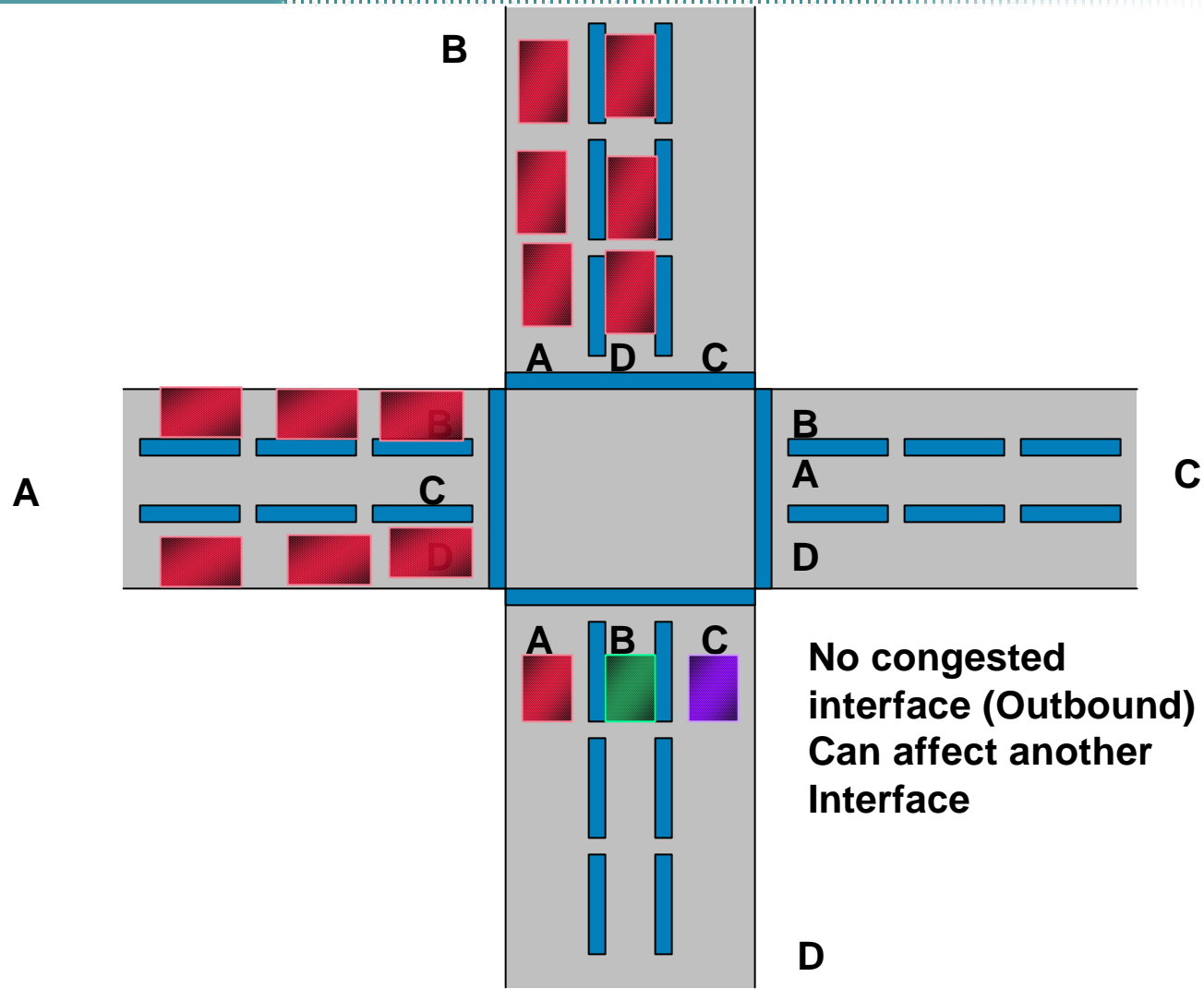
# Single Input FIFO Queue



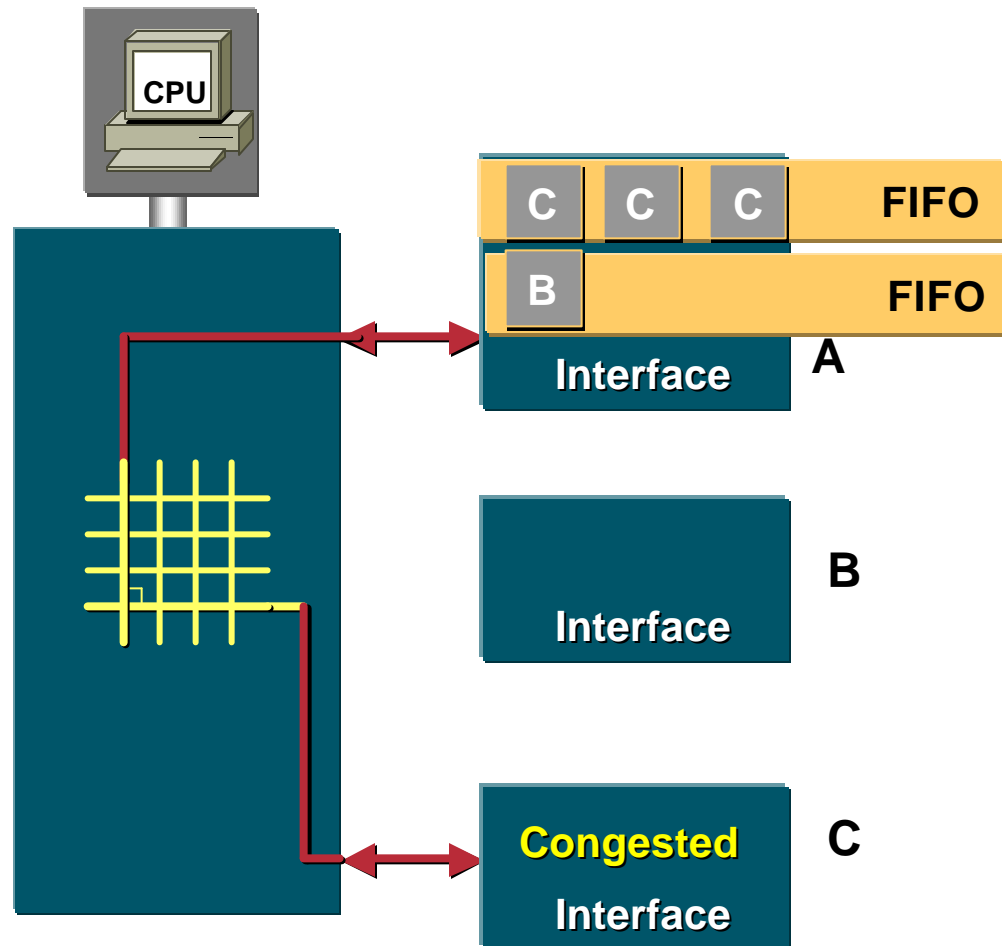
# “Lane Control”



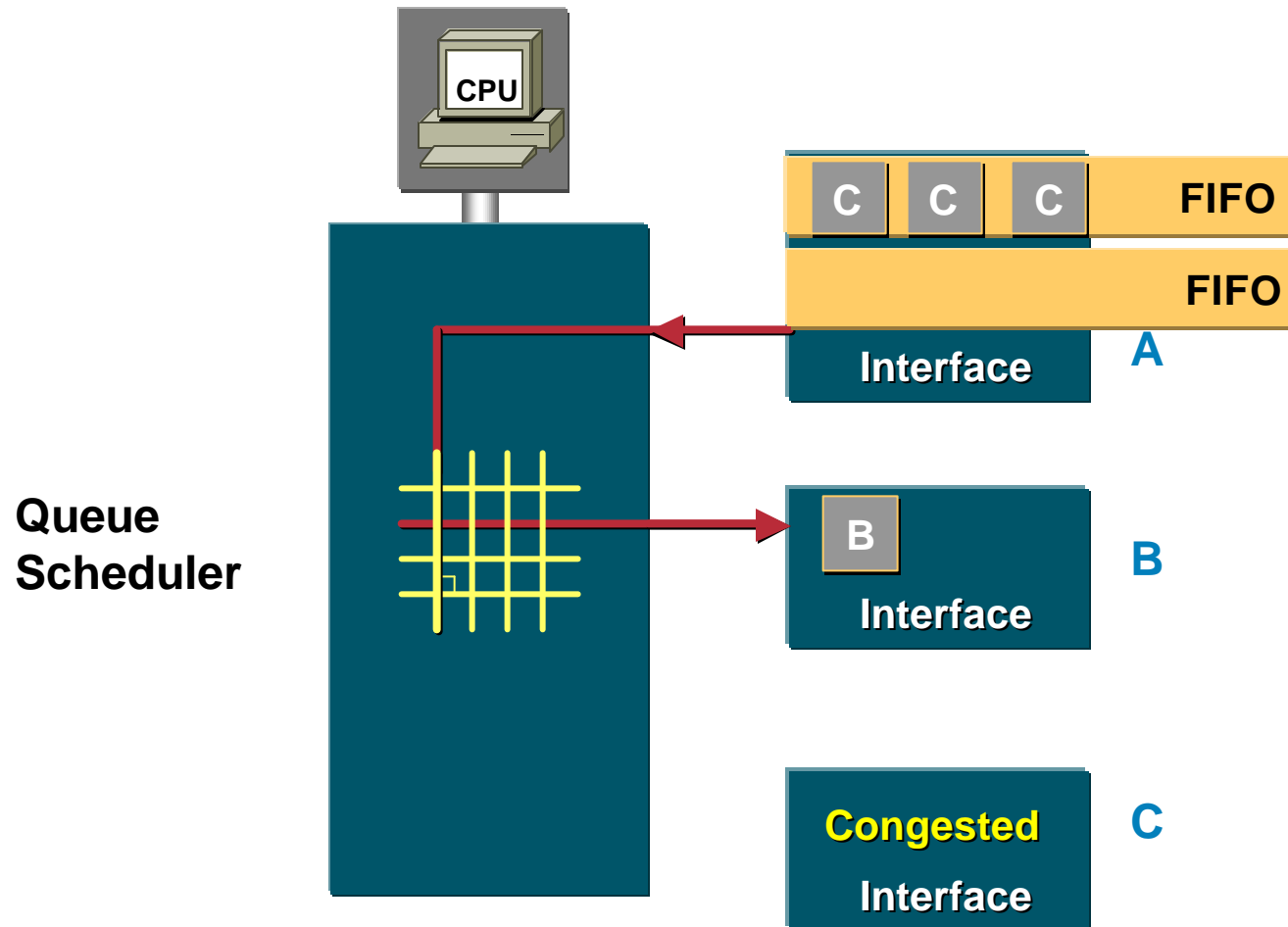
# All Destinations Have a Lane



# Virtual Output Queuing



# Virtual Output Queue



# Components of an Architecture

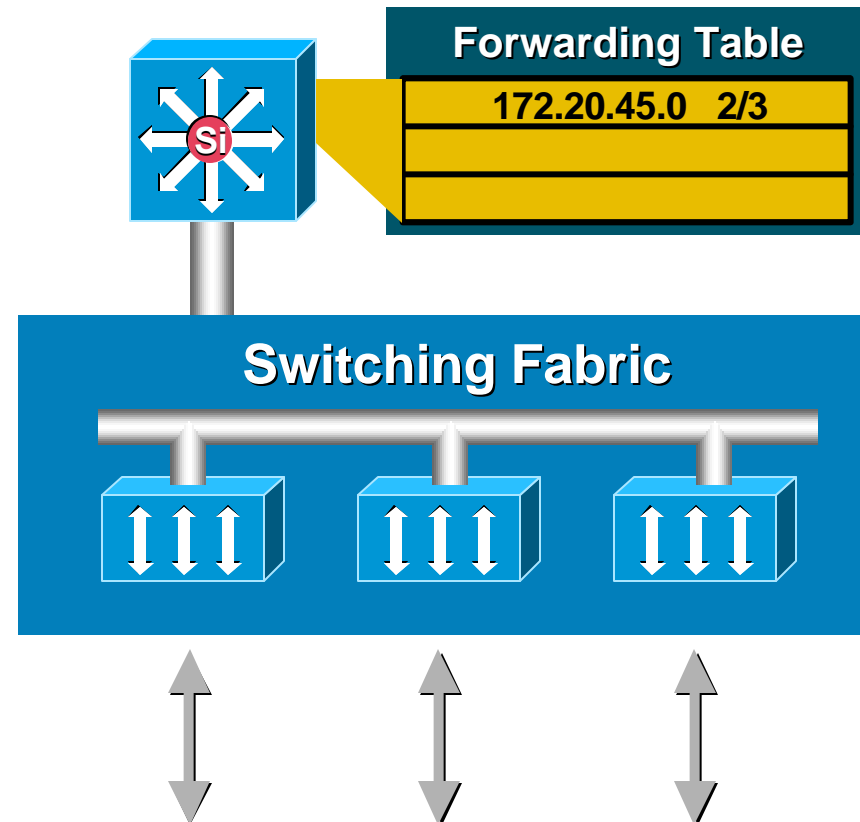
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- **Switching fabric**
- **Memory/buffers**
- **Queuing**
- **Centralized vs. Distributed**
- **Forwarding architectures**

# Centralized Switching

## Central CPU/Switch ASIC

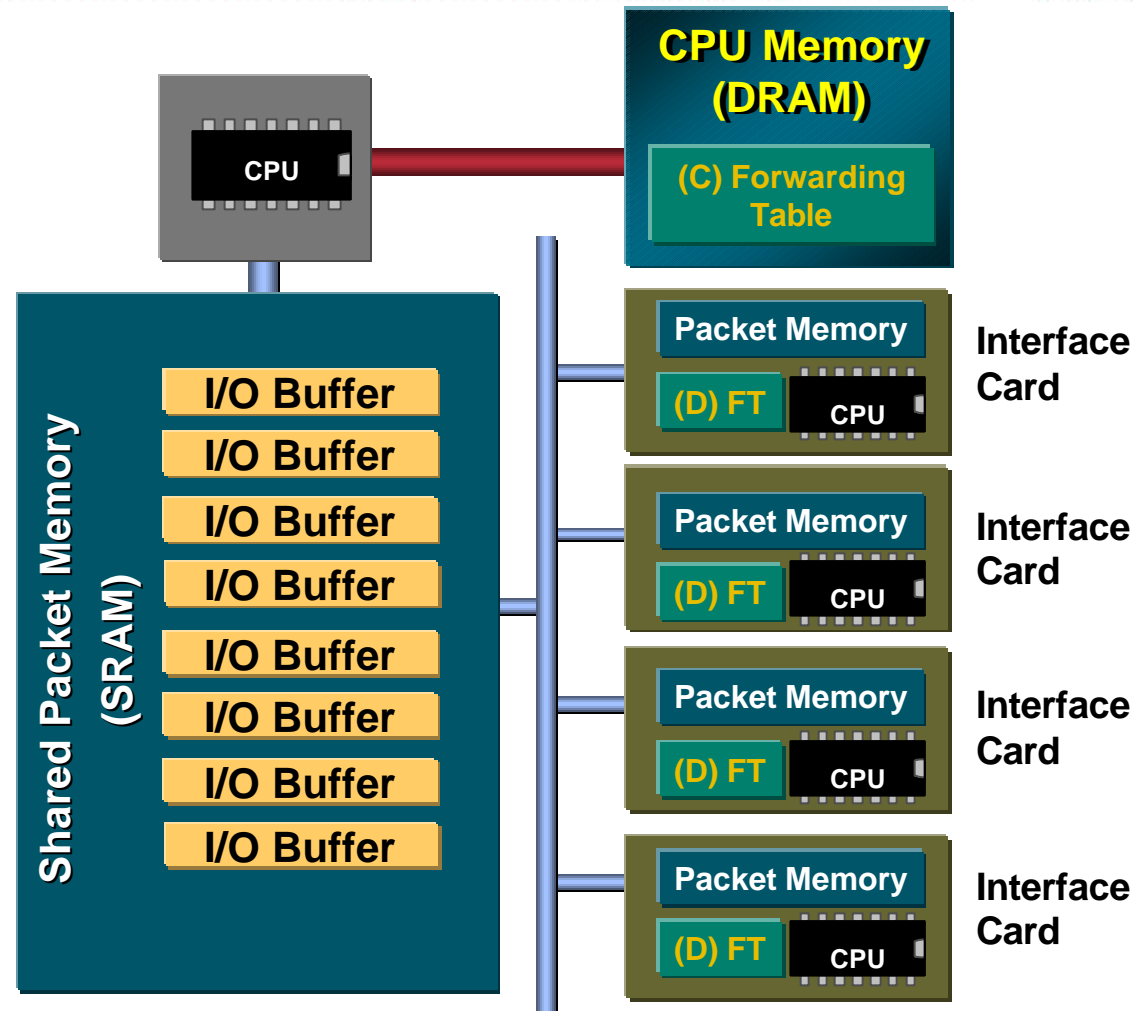
- Central forwarding table utilized
- Provides centralized control for switching and learning
- Lookup can be done in ASICs for faster processing
- Can perform a Layer 2 or Layer 3 lookup



# Distributed Switching

Each Line card has Packet Memory, Forwarding Table Memory and a discrete CPU.

A Copy of the central forwarding table is propagated from the Central Route Processor to the Line Cards for Local switching of packets

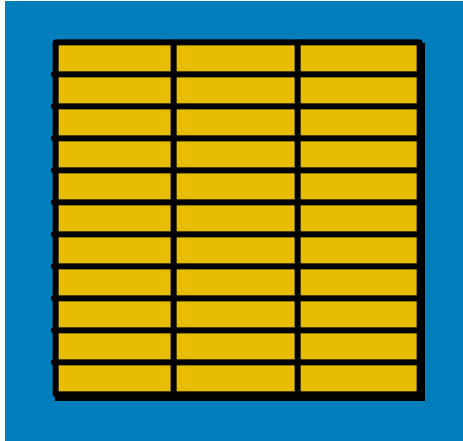


# Components of an Architecture

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- **Switching fabric**
- **Memory/buffers**
- **Queuing**
- **Distributed vs. centralized**
- **Forwarding architectures**

# Serial vs. Hashed Lookup

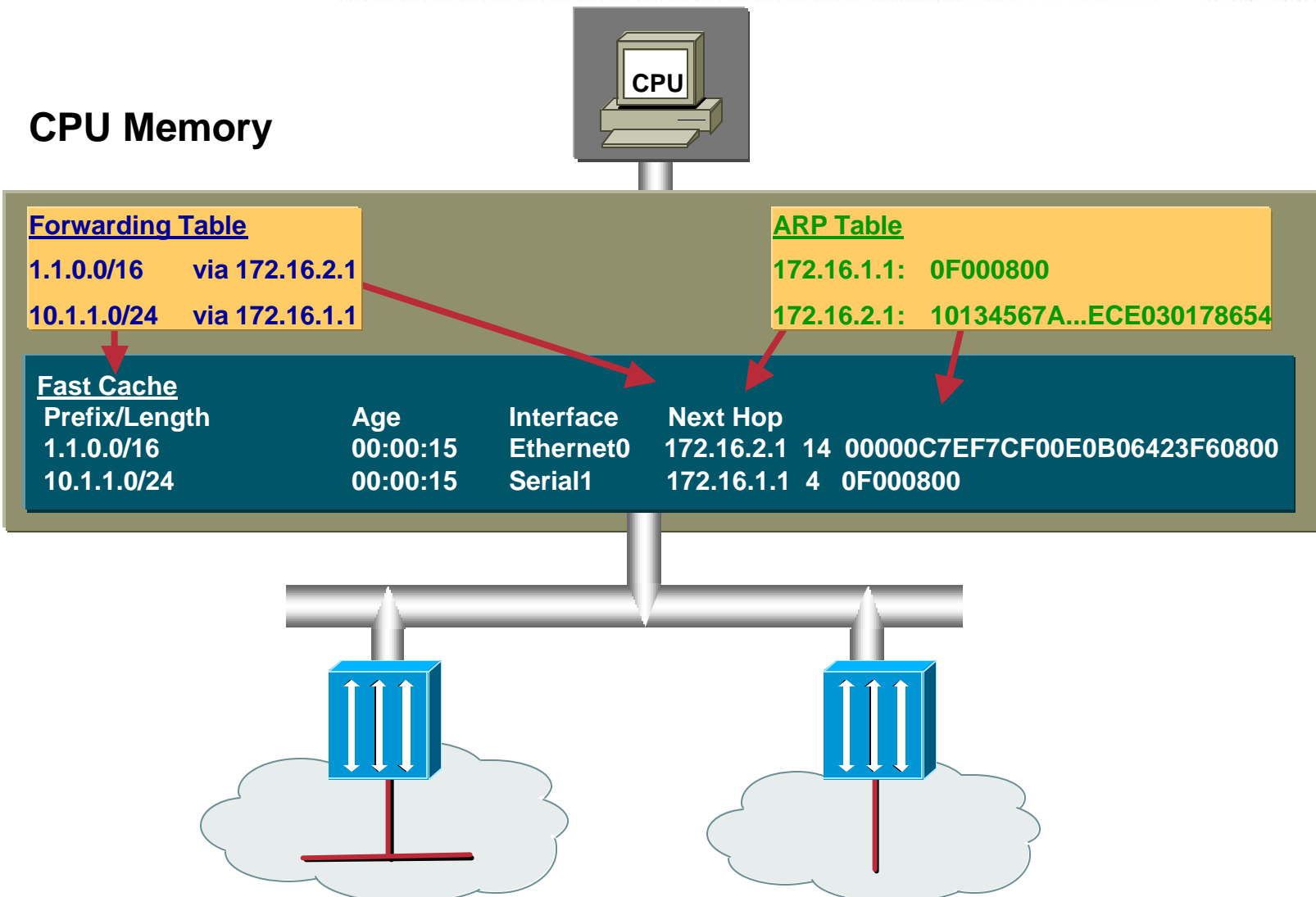


- **Sequentially look up entries in table**
- **Simplistic implementation**

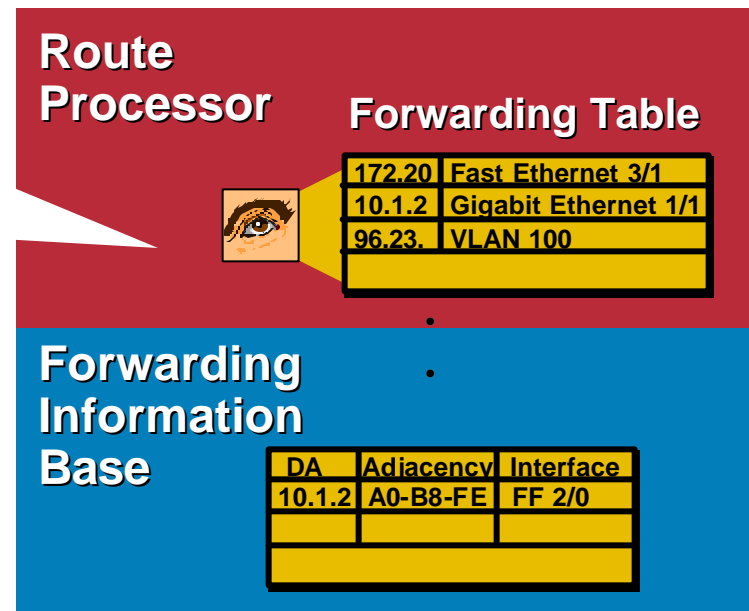
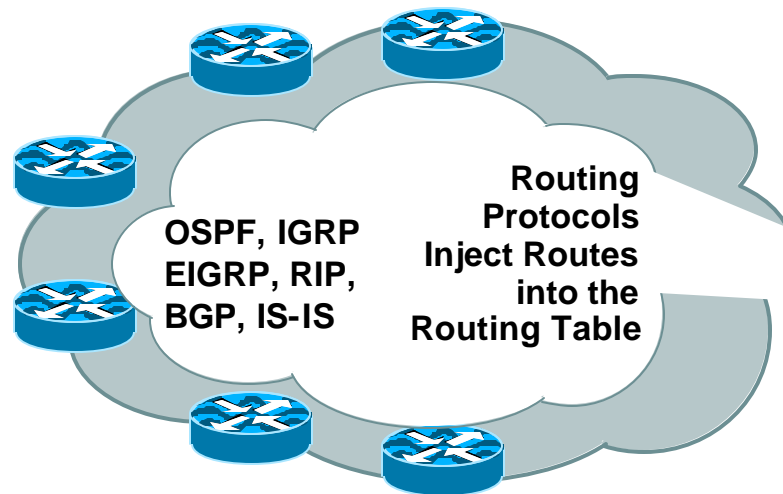


- **Hash values together to obtain a value in memory**
- **Benefit: Faster lookup in larger tables**
- **VLSM causes more overhead and maintenance**

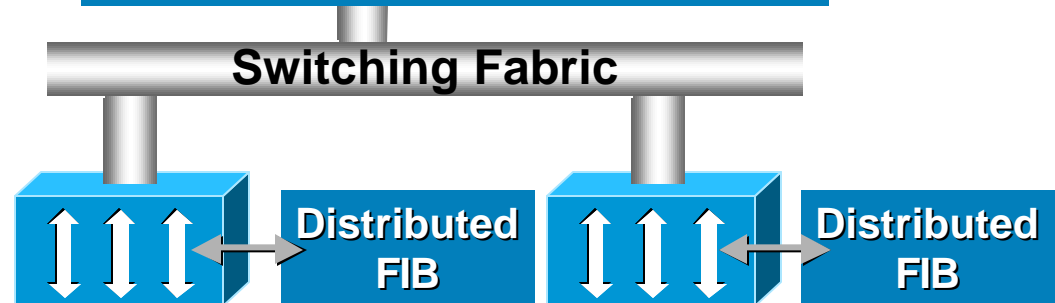
# Demand Generated Cache Based Switching



# Topology-Based Switching

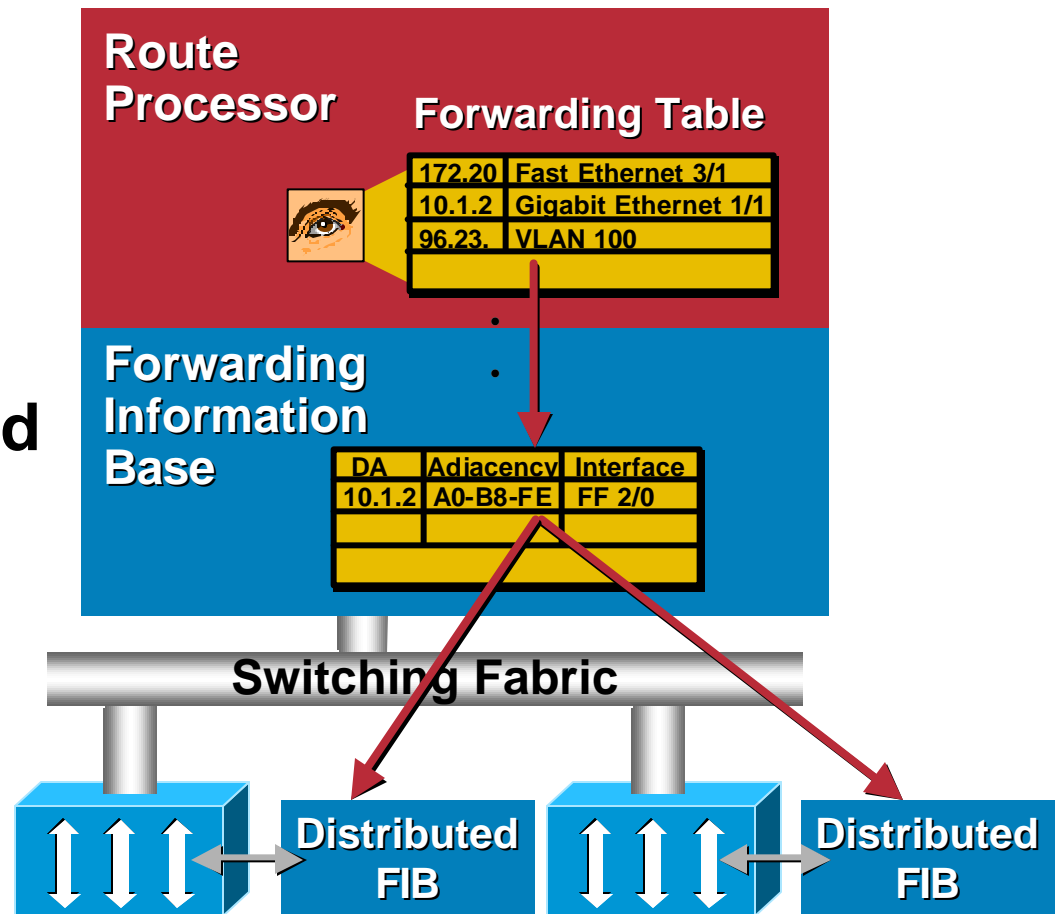


- Forwarding Information Base (FIB)
- Cisco Express Forwarding (CEF)



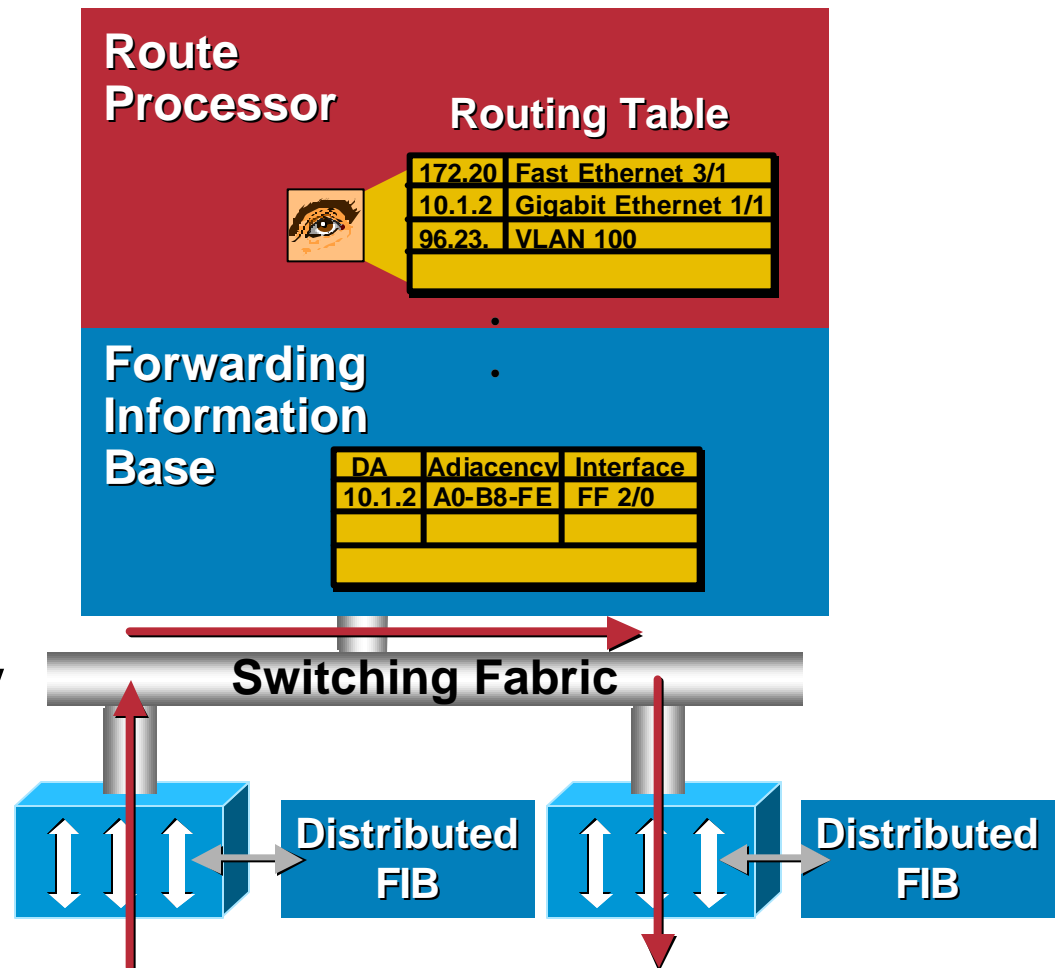
# Topology-Based Switching

- FIB calculated based on routing table entries, not traffic flows
- FIB can be kept central or distributed
- Longest match lookup on prefix/mask
- More scalable for large enterprises and service providers



# Topology-Based Switching

- Packet enters switch
- No process switching necessary
- Decision made locally or centrally regardless of switching fabric

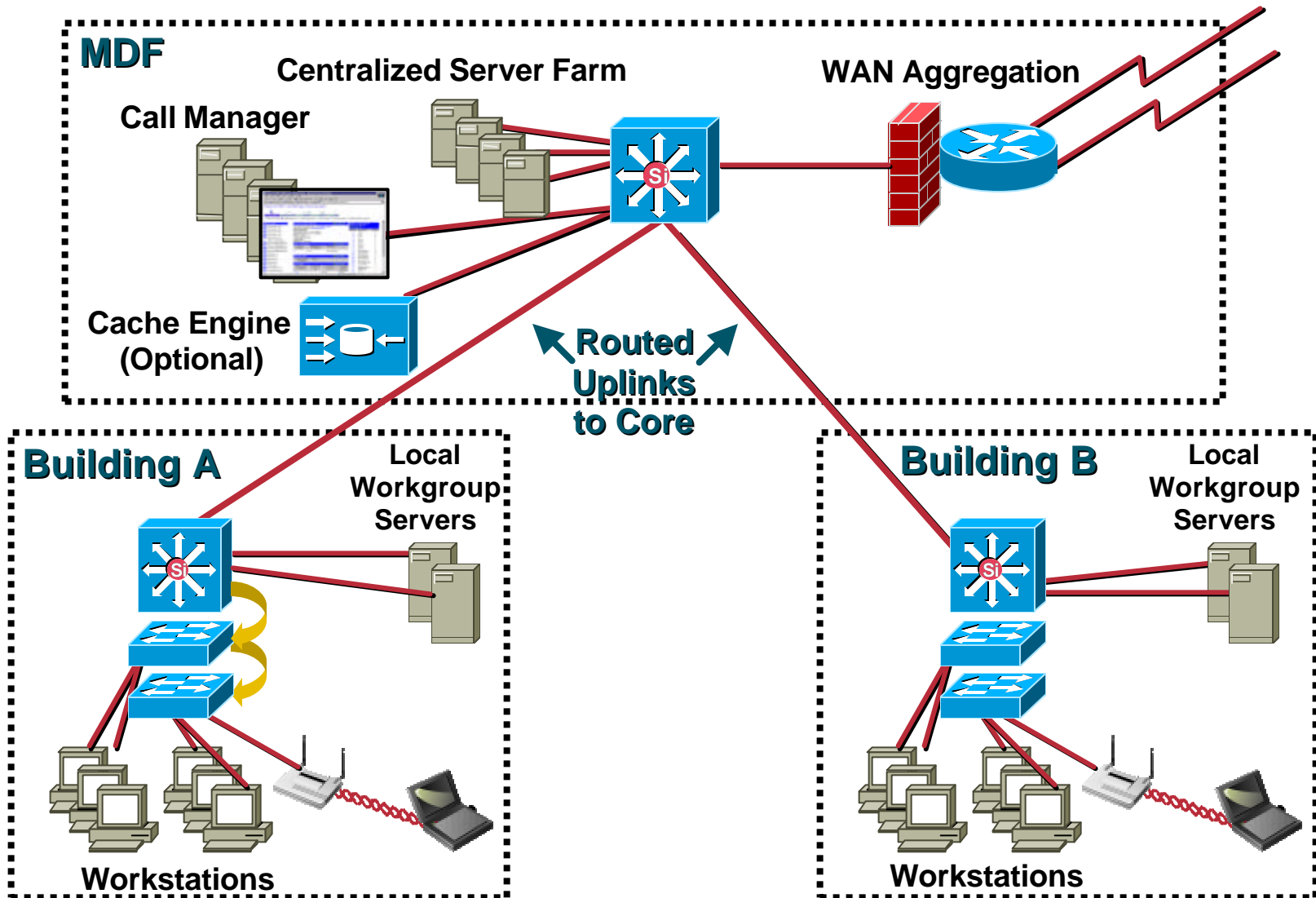


# Summary

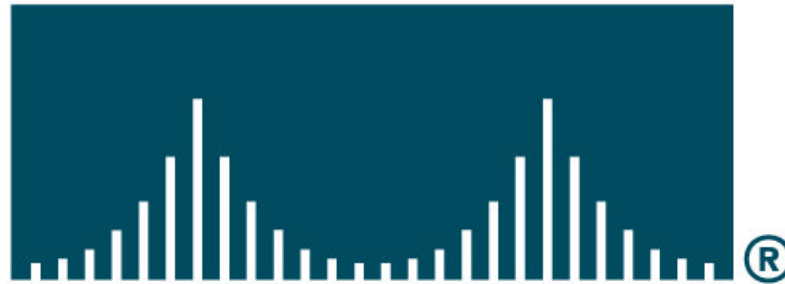
# Summary

- LAN switches and routers use the **same architectural features**
- LAN switches give scalability at **L2**
- Routers give scalability at **L3**
- Deployment of LAN switches and routers in a hierarchical network model offers **scalability, reliability and mobility**

# Network Implementation



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